Synopsys Congratulates Best Paper Award Winners at Its Largest Ever Annual Users Group Conference

Aart de Geus and NASA Principal Scientist Steve Squyres Address Nearly 1,600 Engineers at Seventeenth Annual User's Conference

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MOUNTAIN VIEW, Calif., April 11 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the Best Paper Awards for the 17th annual Synopsys Users' Group (SNUG) in Santa Clara, CA. 'SNUG San Jose' is the largest user's conference in electronic design automation (EDA) and one of the largest gatherings of design engineers in North America. It is the flagship event of a global program that last year drew almost 5,000 chip and system design engineers to 10 such conferences in North America, Europe, Japan and Asia Pacific. This year, a record-breaking 1,574 users attended SNUG San Jose, a 23 percent increase over last year's event. At the technical conference, The Best Paper--First Place and Technical Committee Honorable Mention went to Paul Zimmer of Zimmer Design Systems for "Where Have All the Phases Gone? Using Multiclock Propagation in PrimeTime." The Technical Committee Award went to Eliseu Filho of Starport Systems for "Implementation of an AHB Bus Subsystem with SystemVerilog."

The Best Paper, Second Place Award and Technical Committee Honorable Mention went to Stuart Sutherland of Sutherland HDL, Inc. and Don Mills of LCDM Engineering for "Gotcha Again--More Subtleties in the Verilog and SystemVerilog Standards that Every Engineer Should Know."

The Best Paper, Third Place Award went to Leah Clark of Broadcom Corporation for "Don't Panic! What to do when Formality Doesn't Give You the 'VERIFICATION SUCCEEDED' Message on the First Try."

The Best First Time Presenter Award went to Steven M. Waldstein of Tundra Semiconductor for "How to Verify and Integrate Mixed Signal Third-Party IP."

"SNUG is built on the camaraderie and shared experiences of the attendees," said Andy Copper of ARCH Design Solutions and SNUG San Jose Technical Chairperson. "It strives to set the standard for user conferences by providing a unique environment in which we can meet and discuss technical issues with Synopsys executives, developers and fellow users, and get a glimpse of what innovations are in store."

Aart de Geus, chairman and chief executive officer at Synopsys, gave an opening-day keynote that explained how Synopsys is helping users navigate a design environment of increasing scale and systemic challenges by providing solutions with higher levels of abstraction and increased modeling capabilities. A highlight of the conference was a speech by Steve Squyres, principal scientist for NASA's Mars Exploration Rover Missions. Dr. Squyres told attendees how a team of more than 4,000 highly motivated engineers and scientists overcame a host of technical challenges to develop the Mars Rovers.

"Even in a complex mission such as a Mars landing, you can't lose sight of the technical contributions that are made by engineers like those here at SNUG," said Dr. de Geus. "Complex silicon systems help make planetary exploration possible, and many of the designs at the heart of these systems result from the free exchange of ideas and methodologies. SNUG gives us all a chance to explore ideas like these, and to consider solutions to current and future technical challenges. We congratulate this year's Best Paper Award winners and thank them for sharing their technical knowledge and experiences with fellow users."

SNUG San Jose Sponsors include: Global Sponsors ARM and TSMC; Gold Sponsors Hewlett-Packard, Virage Logic, and Common Platform Technology members Chartered Semiconductor, IBM and Samsung; and Silver Sponsor Sun Microsystems. The three-day SNUG San Jose conference featured 52 technical presentations, 36 tutorials and 14 panels, all presented by Synopsys users and experts to fellow design engineers. These presentations focused on the challenges that engineers face as they design complex systems for a wide array of applications. Two new types of sessions, delivered by Synopsys technologists, were introduced at this year's event. Product Direction Panels offered a sneak peek at what Synopsys is doing in the verification, implementation, analog/mixed signal and design for manufacturing (DFM) arenas. Technology Vision sessions explored the future of the EDA industry in two key areas: low power and system-to-silicon verification. Synopsys also launched a new micro-site during the event: http://www.socdesignsource.org/ offers the latest information and resources for low-power design.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com.

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