Synopsys DesignWare IP to Enable Next-Generation PCI Express 2.0 Products

Synopsys Is First to Deliver PCI Express Gen II Digital IP for Increased Bandwidth in Networking, Embedded and Computer Applications

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that its portfolio of DesignWare® digital controller IP for PCI Express™ is the first to support the evolving 2.0 version (Gen II) of the PCI Express specification. The portfolio includes Endpoint, Root Complex, Switch, Bridge and Dual Mode Cores. While maintaining backward compatibility with the 1.1 version of the specification, the Gen II specification provides several improvements, including an increase to 5 gigabits per second data rate to address the industry's need for increased bandwidth in networking, embedded and computer applications. Synopsys, an active member of the PCI Special Interest Group (PCI-SIG), currently supports the latest (0.7) revision of the Gen II specification and will deliver updates to track the specification as it evolves. This early availability enables companies to begin product development immediately and help deliver compliant products close to the release of the final Gen II specification.

"We chose the DesignWare IP for PCI Express because of Synopsys' aggressive support for the 2.0 standard, their track record of delivering quality IP, and their excellent customer service," said George Hopkins, director of Engineering at SGI. "We have been working with Synopsys' DesignWare IP for PCI Express 2.0 since the 0.3 version of the specification, which has enabled us to immediately integrate new features into products under development. This helps us ensure that we meet our customers' demand for products requiring ever-increasing bandwidth."

"As the leader in PCI Express IP, we understand the importance of making Gen II available to our customers as soon as possible. For this reason, we are releasing the cores early, before the specification is finalized," said Guri Stark, vice president of Marketing, Solutions Group at Synopsys. "Early support for PCI Express 2.0 addresses our customers' time-to-market and reinforces Synopsys' commitment to supporting emerging standards that impact our customers' design needs and critical market windows."

Availability

The DesignWare digital controller cores for PCI Express IP 2.0 are available now for early adopters. The DesignWare Verification IP for PCI Express 2.0 is scheduled for general availability in Q1 of calendar 2006.

About DesignWare Cores

Synopsys DesignWare Cores provide system designers with silicon-proven, digital, and mixed-signal connectivity IP for some of the world's most recognized products, including communications processors, routers, switches, game consoles, digital cameras, computers, and computer peripherals. Provided as synthesizable RTL source code or in GDS format, these cores enable designers to create innovative, cost-effective systems-on-chips and embedded systems. Synopsys provides flexible licensing options for the DesignWare Cores. Each core can be licensed individually, on a fee-per-project basis, or users can opt for the Volume Purchase Agreement, which enables them to license all the cores as part of one simple agreement. For more information on DesignWare IP, visit: http://www.designware.com/ .

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits of the DesignWare digital controller IP for PCI Express and the expected commercial release date for the DesignWare Verification IP for PCI Express 2.0. These statements are based on current expectations and

beliefs. Actual results could differ materially from these statements as a result of (i) unforeseen difficulties by customers in incorporating the controller IP into their designs prior to completion of the PCI Express 2.0 specification, (ii) uncertainties attendant to any new technology offering and (iii) certain statements contained in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2005 entitled "Management's Discussion and Analysis of Financial Condition and Results of Operations - Factors That May Affect Future Results."

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