Synopsys PrimeYield LCC Links to IC Compiler for Automated Correction of Lithography Problems

Toshiba to Deploy Integrated, Production-Proven DFM Technology into Standard Layout Flow

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that PrimeYield -- the company's new, comprehensive tool suite for design-yield analysis -- enables automated correction of manufacturing problems early in the design process. Announced today (see "Synopsys Extends DFM Leadership with Launch of PrimeYield Tool Suite for Yield Analysis"), PrimeYield integrates design with manufacturing by accurately predicting design-induced mechanisms that threaten yield and by providing automated correction guidance to upstream design implementation tools. The lithography compliance-checking (LCC) module within PrimeYield tightly links to Synopsys' IC Compiler advanced physical implementation solution, enabling fast detection and correction of litho-related issues for 65 nanometer (nm) and smaller chip designs.

"Design-team productivity is imperative to us," said Yukihito Oowaki, Senior Manager System LSI Design Dept., Toshiba Corporation Semiconductor Company. "Synopsys' PrimeYield LCC provides an automatic and seamless method for us to detect lithography problems and deliver correction guidance to our place-and-route environment, IC Compiler. We are very excited about the efficiency and accuracy of Synopsys' PrimeYield LCC technology and will be deploying it into our standard layout flow."

PrimeYield gives designers a preview of the issues that will impact the manufacturability of their devices at 65nm and below advanced technology nodes. PrimeYield addresses these issues via its three core modules -- LCC; model-based chemical-mechanical polishing (CMP) checking; and critical area analysis (CAA) -- providing designers with the critical toolset they need to correct and modify the design before tapeout.

PrimeYield's tight links to design implementation enable it to drive automatic correction within IC Compiler and accurate parasitic extraction within the Star-RCXT™ tool. Variation-aware extensions of Synopsys' gold-standard PrimeTime® static timing analysis and Star-RCXT extraction tools were also announced today, further strengthening the link between design and manufacturing to help customers improve design robustness and parametric yield at 65nm and below.

IC Compiler is an advanced physical implementation solution with everything necessary to do next-generation designs, including physical synthesis, placement, routing, timing, signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization. IC Compiler provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure.

"With the introduction of PrimeYield, Synopsys delivers an automated solution that both identifies and fixes manufacturing problems," said Raul Camposano, Synopsys' chief technology officer, senior vice president and general manager of the Silicon Engineering Group. "This makes PrimeYield LCC's link to IC Compiler extremely valuable for increasing designers' efficiency and helping accelerate time to entitled yield for leading chipmakers such as Toshiba."

About Synopsys DFM

With its DFM tools, Synopsys is expanding on what is already the industry's most comprehensive design for manufacturing (DFM) solution that spans from RTL to silicon. Synopsys' DFM product family addresses critical manufacturability and yield issues with the following products: IC Compiler physical design solution, PrimeYield LCC, PrimeYield CMP and PrimeYield CAA technologies, Hercules™ physical verification tool, Proteus OPC, CATS® mask data preparation product, SiVL® lithography verification tool, patented PSM technology, and physics-based TCAD suite of simulation products. Synopsys' Manufacturing Yield Management (MYM) solutions extend directly into the fab, providing customers real time access to yield data and the analysis capability needed to reduce random, systematic and parametric defects.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the

design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the anticipated benefits of Synopsys' PrimeYield tool suite. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties of customers in deploying the tool suite, uncertainties attendant to any new product offering and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended April 30, 2006 entitled "Management's Discussion and Analysis of Financial Condition and Results of Operations - Factors That May Affect Future Results."

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 x115
lgmartin@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635 or sgulizia@synopsys.com; or Lisa Gillette-Martin of MCA, Inc., +1-650-968-8900, ext. 115, or lgmartin@mcapr.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/