Synopsys Introduces Industry's First 90 Nanometer USB 2.0 On-The-Go PHY and Extends Its Hi-Speed USB PHY to 90 Nanometer Node

Silicon-Proven PHY Cores Expand Industry-Leading DesignWare USB IP Portfolio

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Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced the availability of the DesignWare® USB 2.0 On-The-Go (OTG) PHY (Physical Layer) Core targeted to TSMC's 90 nanometer (nm), 130-nm and 180-nm processes as well as an extension of the Hi-Speed USB 2.0 PHY Core product line to the 90-nm process node. The DesignWare USB 2.0 OTG PHY is the industry's first 90-nm USB OTG PHY Core. The DesignWare USB 2.0 OTG PHY is interoperability tested and jointly certified with Synopsys industry leading digital USB cores, thus providing a complete drop-in solution with lower cost, form factor and risk.

These 90-nm product introductions complement Synopsys' certified Hi-Speed USB 2.0 PHYs currently in volume production on TSMC's 180-nm and 130-nm processes. The new USB PHYs, which are complete physical layer interface cores compliant with the USB 2.0 OTG standard that provide an integrated solution that has been implemented in silicon and tested with Synopsys' leading family of digital USB intellectual property (IP) cores, including the DesignWare Hi- Speed OTG controller, Host Controller and Device Controllers.

The new OTG PHY handles HNP (host negotiation protocol) and SRP (session request protocol), which are the OTG-specific differences between the Hi-Speed 2.0 and the new OTG standard. Available targeted to TSMC's 180-nm, 130-nm and 90-nm processes, the OTG solution is based on the Synopsys USB 2.0 PHY that is already certified and shipping in volume.

USB OTG is a supplement to the USB 2.0 specification that increases the capability of existing mobile devices and USB peripherals by adding host functionality for connections to USB peripherals. Many of the new peripherals connected to PCs and laptops are portable devices. As these portable devices increase in popularity, there is a growing need for them to communicate directly with each other when a PC is not available. The OTG supplement addresses this need for mobile inter-connectivity and defines a way for portable devices, through only one mini-connector, to connect to supported USB products in addition to the PC.

"With the introduction of our USB 2.0 OTG PHY, designers can speed integration and reduce risk when designing a complete digital and mixed-signal OTG solution targeted to TSMC's most popular foundry processes," said Guri Stark, Synopsys' vice president of Marketing, Solutions Group. "For designers at the leading edge of system design, our Hi-Speed USB 2.0 PHY and USB 2.0 OTG PHY in TSMC's 90-nm process enable them to achieve USB 2.0 connectivity based on our USB-certified PHY architectures proven at 180-nm and 130-nm. Our complementary DesignWare USB PHY and digital IP solutions give designers a one-stop shop and help them lower design risk with proven, interoperable solutions."

Pricing and Availability The DesignWare USB OTG PHYs and Hi-Speed USB 2.0 PHYs are available now for TSMC's 180-nm, 130-nm and 90-nm processes. These PHYs are also available for porting to additional foundry processes. Contact Synopsys for pricing information.

About DesignWare Cores

DesignWare Cores provide system designers with silicon proven, digital and analog connectivity IP for some of the world's most recognized products including communications processors, routers, switches, game consoles, digital cameras, computers and computer peripherals. The DesignWare IP family includes industry leading connectivity IP Cores and Verification IP (e.g., USB 1.1, USB 2.0, USB 2.0 PHY, USB 2.0 OTG, USB 2.0 OTG PHY, PCI, PCI-X®, PCI Express™, Ethernet...), AMBA™ on-chip bus (logic, peripherals, verification IP) and microcontrollers (8051, 6811). Provided as synthesizable RTL source code or in GDS format, these cores enable designers to create innovative, cost-effective systems-on-chip and embedded systems. Synopsys provides flexible licensing options for the DesignWare Cores. Each Core can be licensed individually, on a fee-per-project basis or users can opt for the Volume Purchase Agreement, which enables them to license all the cores under one simple agreement. For more information on DesignWare IP, visit www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC

manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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