Synopsys Delivers Galaxy 2004 With 2x Performance, 2x Capacity and 2x Yield Enhancement Features

Galaxy 2004 Accelerates Design Convergence Through Correlation With Sign-Off in the Platform

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.

Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced the release of Galaxy™ 2004, a major upgrade to its complete design platform that delivers across-the-board improvements in run-time, capacity, quality-of-results (QoR), silicon technology support and turn-around time. These improvements impact virtually every stage of the design flow through the Galaxy Design Platform, including RTL synthesis, design planning, power management, signal integrity, testability, placement, routing, sign-off, physical verification and yield enhancement. Extensive advancements have been made to improve timing correlation throughout all stages of the implementation flow and the industry-standard sign-off tools, PrimeTime® and Star-RCXT™. All tools in the Galaxy platform now use identical constraints, libraries and delay calculation to facilitate rapid design convergence.

"The vast range of advancements in Galaxy 2004 demonstrates the tremendous rate at which Synopsys is innovating to produce the most convergent flow for SoC design," said Aart de Geus, chairman and CEO at Synopsys. "Galaxy 2004 represents a big step forward in design technology, providing the fastest path to the best results, which are highly correlated to silicon."

Numerous innovations in Galaxy 2004 contribute to significant performance improvements throughout the entire flow. Design Compiler® 2004 posts two times faster run-time, 40 percent better capacity and 10 percent better area QoR than last year's release. Design Compiler benefits from a greatly simplified synthesis flow that enables designers to run a top-down compile for large blocks on a 32-bit workstation, resulting in even greater runtime improvements. Design Compiler now also supports SystemVerilog and a new VHDL Compiler that is five times faster and has broader language coverage than its predecessor.

Synopsys' JupiterXT™ design planning solution in Galaxy 2004 has also been greatly enhanced, with twice the capacity of last year's version and up to three times speed improvement in time required to create a detailed floorplan. JupiterXT also features a fast feasibility mode, enabled by its virtual flat design planning capability, a completely new automatic macro placement capability based on Synopsys' patented placement technology, power plan synthesis, and a highly predictive capability for power network analysis (PNA). The PNA capability enables IR-drop analysis at the floorplan level with high correlation to final IR-drop sign-off in Astro-Rail™. This solution also drives PrimeTime SI to enable voltage-drop dependent timing sign-off.

In the Physical Design area, both Physical Compiler® and Astro™ have been improved. Physical Compiler now has two times faster run-time, two times better capacity and 15 percent better timing QoR than last year's version. Physical Compiler also includes a new Distributed Physical Synthesis capability, which distributes large flat designs over multiple CPUs for fast turn-around time, and performs a final global optimization for best quality of results. Physical Compiler also includes a new capability for significant congestion removal without degrading timing results. Astro now has 50 percent better capacity, TCL command-line support, simpler library preparation and a new easy-to-use recommended methodology that achieves high QoR without complex scripting. In physical verification, Hercules™ Physical Verification Suite (PVS) now has two times faster runtime, industry-leading distributed processing delivering an additional five times faster turn-around on just six CPUs, and foundry-qualified optimized runsets available from all major foundries.

Galaxy 2004 also delivers significant new features for improving yield. Astro now includes automatic timing-driven wire spreading for uniform wire density, as well as automatic via optimization and redundant via insertion without increasing area or congestion. Additionally, Astro provides automatic timing-driven dummy metal fill insertion to avoid placing metal fill near critical paths. Hercules introduces enhanced commands for more efficient DFM checking, such as advanced via array spacing, width-based metal spacing, and min-max density checking. Furthermore, Hercules now supports enhanced device extraction features such as length-of-diffusion (LoD) parameter extraction for the accurate modeling of shallow-trench-isolation effects, a critical yield factor for 90-nanometer design.

PrimeTime, Synopsys' industry-standard timing sign-off solution, now has three times improvement in both runtime and capacity. In addition, PrimeTime now supports instance- and net-specific timing derating for improved support of on-chip variation. PrimeTime SI, Synopsys' signal integrity (SI) analysis and sign-off solution, now offers improvements in usability with new reporting and diagnostics for SI violations and increased accuracy with path-based analysis. Star-RCXT, industry-leading parasitic extraction solution, now has up to two times improvement in both runtime and capacity.

In the testability area, DFT Compiler™ is now two to five times faster, has two times the capacity and features timing-based physical scan ordering in Physical Compiler. TetraMAX® ATPG is now two to three times faster, produces three times fewer test patterns, and now fully automates Phase-Locked Loops (PLLs) and internal clock control to provide a complete solution for at-speed testing. TetraMAX is also the first commercial tool that directly uses physical layout information to specifically target bridging defects.

Galaxy 2004 also extends Synopsys' lead in power management and reliability. Power Compiler™ now provides support for power-gating retention registers, enabling very high leakage power savings in power-down mode for multi-mode designs. PrimePower, Synopsys' accurate gate-level power analysis tool, introduces vector-free power analysis using integrated PrimeTime technology. Astro-Rail, an SoC reliability analysis tool, adds "what-if" capabilities for voltage-drop and electro-migration trade-off analysis.

Availability

The 2004.06 version of Galaxy Design Platform is expected to be made available to customers via two releases in June and July of 2004.

About Galaxy Design Platform

The Galaxy Design Platform is an open, integrated design implementation platform with best-in-class tools and IP, enabling advanced semiconductor design. Anchored by Synopsys' industry-leading semiconductor design tools and the open Milkyway™ database, the Galaxy Design Platform incorporates consistent timing, SI analysis, common libraries, delay calculation, constraints, testability, and physical verification to provide a convergent flow from RTL all the way to silicon. The Galaxy Design Platform helps reduce design time, decrease integration costs and minimize the risks inherent in advanced, complex semiconductor design.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

SOURCE: Synopsys, Inc.

CONTACT: Robert Smith of Synopsys, Inc., +1-650-584-1261, or rsmith@synopsys.com; or Sarah Seifert of Edelman, +1-650-968-4033, or sarah.seifert@edelman.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/