Synopsys Announces Support for SUSE LINUX With Galaxy Design and Discovery Verification Platforms

Customers Gain Access to EDA Industry's Most Extensive Linux Support

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, announced it will support the SUSE® LINUX Enterprise Server 9 operating system (OS) from Novell® on both 32-bit and 64-bit x86 instruction sets for Synopsys' Galaxy™ Design and Discovery™ Verification Platforms. Running on Novell's SUSE LINUX Enterprise Server 9, Synopsys' technology now offers design and verification engineers performance and scalability with an even greater choice of Linux operating systems.

"We applaud Synopsys for today's announcement," said Karla Reynolds, director of CAD at AMI Semiconductor (AMIS). "Given the rapid advancement of the SUSE Linux distribution, it is important to us that software vendors recognize the value of delivering stable products to run on it. We have successfully run a wide range of Synopsys products on SUSE Linux for many years at AMIS, and by certifying SUSE LINUX Enterprise Server 9, Synopsys provides us added flexibility."

"The certification of Novell's SUSE LINUX Enterprise Server 9 with Synopsys' EDA software confirms the power of Linux in the enterprise," said David Patrick, general manager, Linux and Open Source of Novell. "Synopsys is a company known for endorsing well-supported platforms offering their customers extremely high performance, capacity, reliability, and cost-effectiveness. Novell is excited that SUSE LINUX Enterprise Server 9 enables Synopsys to offer Linux for EDA, opening up more choice for customers."

"We continually update our compute platform support for Synopsys' Galaxy and Discovery technology to address customers' needs for stable and well-supported operating systems. Adding Novell's SUSE LINUX Enterprise Server 9 to our roadmap demonstrates Synopsys' commitment to serving our customers," said Karen Bartleson, director of Interoperability at Synopsys.

Synopsys support for Novell's SUSE LINUX Enterprise Server 9 is scheduled for delivery to customers in the first quarter of 2005. The Galaxy and Discovery platform tools to support SUSE LINUX Enterprise Server 9 will include: The Design Compiler® family products used for RTL synthesis, DesignWare® Library arithmetic generators and building blocks used for synthesis; DFT Compiler™ and TetraMAX® test tools; Physical Compiler®, JupiterXT™ and the Astro™ family of products used for physical implementation; Power Compiler™ power management software; PrimeTime® and PathMill® static timing analysis tools; HSPICE® circuit simulator tools; Hercules™ layout verification solution; NanoSim® mixed-signal design product; Proteus tool for full-chip proximity correction, Star-RCXT full-chip parasitic extraction tool and CATS® mask data preparation software. Further product support in the third quarter of 2005 is planned to add the VCS® comprehensive RTL verification solution, DesignWare Verification Library, ESP and Formality® equivalency checking solutions.

About Galaxy Design Platform

The Galaxy Design Platform is an open, integrated design implementation platform with best-in class tools and IP, enabling advanced semiconductor design. Anchored by Synopsys' industry-leading semiconductor design tools and the open Milkyway™ database, the Galaxy Design Platform incorporates consistent timing, SI analysis, common libraries, delay calculation, constraints, testability, and physical verification to provide a convergent flow from RTL all the way to silicon. The Galaxy Design Platform helps reduce design time, decrease integration costs and minimize the risks inherent in advanced, complex semiconductor design.

About Discovery Verification Platform

The Discovery Verification Platform is a unified environment that provides high performance and efficiency of interaction among all platform components, including mixed-HDL simulation, mixed-signal, system-level verification, assertions, verification intellectual property, code coverage, functional coverage, testbenches and formal analysis. Combined with SystemVerilog and Synopsys' design-for-verification methodology, the Discovery Verification Platform helps designers achieve higher levels of verification productivity by contributing to first-time silicon success within required project cycles.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex

systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

NOTE: Synopsys, CATS, Design Compiler, DesignWare, Formality, HSPICE, NanoSim, PathMill, Physical Compiler, PrimeTime, TetraMAX and VCS are registered trademarks of Synopsys, Inc. Astro, DFT Compiler, Discovery, Galaxy, Hercules, JupiterXT, Milkyway, Power Compiler and Star-RCXT are trademarks of Synopsys. All other products mentioned in this release are the intellectual property of their respective owners.

SOURCE: Synopsys, Inc.

CONTACT: Pierre Golde of Synopsys, Inc., +1-650-584-4194, or golde@synopsys.com; or Suraya Akbarzad of Edelman Public Relations, +1-650-429-2757, or suraya.akbarzad@edelman.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/