Synopsys to Release a Complete, Single Vendor Interface IP for High-Performance DDR2 SDRAM Memory Subsystems

Complete Solution Will Include Memory Controller and Mixed-Signal PHY to Reduce Risk and Speed System Integration

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that it will expand its DesignWare® Cores intellectual property (IP) with the planned release of a single vendor, complete system-level interface solution for high-performance DDR2 SDRAM memory subsystems. The new DesignWare IP will help ensure overall memory system performance of up to 800 megabits per second (Mbps) by delivering a complete DDR2 SDRAM memory interface solution that includes a scalable digital controller, a complete integrated physical interface hard macro and verification IP that supports state-of-the-art verification methods. Seamless integration between memory controller and PHY minimizes risk and maximizes performance. It also reduces overall system latency and enables more predictable success for designers using high-performance DDR2 SDRAM technology. The matching verification IP provides full support for VCS® Native Testbench for up to five-times faster verification performance, and further reduces the IP integration and system-level verification effort.

High-performance DDR2 SDRAM is an increasingly common memory solution for designs requiring improved data bandwidth capabilities, lower power and enhanced signaling features. However, the benefits of DDR2 SDRAM are coupled with significant physical implementation challenges that limit performance and increase the cost of implementation. Designers can spend a considerable amount of time managing integration and signaling details when implementing high-performance DDR2 SDRAM interfaces and IP acquired from multiple vendors. This situation increases design risk and may ultimately compromise the system's performance, especially at speeds of up to 800 Mbps.

With Synopsys' complete DesignWare DDR2 SDRAM solution, customers will be able to implement a proven, reliable high-performance complex memory interface in significantly less time than using discrete components allows. In addition, customers will benefit from the added level of system-level test, power management and signaling optimization not easily achieved using discrete memory interface IP components. The DesignWare DDR2 Memory Controllers offer distinct solutions targeted for a wide range of applications, from lean and efficient DDR2 protocol translations to full-featured multi-port with optimized scheduling operation.

The DesignWare Mixed-Signal DDR2 SDRAM PHY and DesignWare Cores DDR2 SDRAM Memory controller solutions will deliver predictable performance and increased margins, and will help considerably reduce implementation and integration time. Developed as a complete system-level interface IP solution, the DesignWare DDR2 SDRAM solution is designed to operate reliably across multiple interconnect topologies and packaging technologies.

"By providing a complete DDR2 SDRAM interface IP solution for our customers, we will significantly reduce the onerous and risky task of integrating discrete memory subsystem IP components. We will also reduce the interoperability challenges associated with the controller/PHY boundary," said Guri Stark, vice president of Marketing for the Solutions Group at Synopsys. "Solving these problems helps our customers concentrate on value-added portions of their designs instead of spending time trying to develop a high-performance DDR2 SDRAM memory subsystem. This ultimately saves design time and helps ensure that performance goals will be met."

Availability

Synopsys' DesignWare DDR2 SDRAM Memory Controller and Mixed-Signal PHY are expected to be available in Q1 of calendar 2007. The DDR2 memory model and AXI™ verification IP are included in the DesignWare Library and the VCS Verification Library and are available immediately. For more information on the DDR2 SDRAM Interface IP Complete Solution, visit: https://www.synopsys.com/designware-ip/interface-ip/ddrn.html

About DesignWare Cores

Synopsys DesignWare Cores provide system designers with silicon-proven, digital, and mixed-signal connectivity IP for some of the world's most recognized products, including communications processors, routers, switches, game consoles, digital cameras, computers and computer peripherals. Provided as synthesizable RTL source code, or in GDS format, these cores enable designers to create innovative, cost-effective system-on-chips and embedded systems. Synopsys provides flexible licensing options for the

DesignWare Cores. Each core can be licensed individually on a fee-per-project basis, or users can opt for the Purchase Agreement, which enables them to license all the cores as part of one simple agreement. For more information on DesignWare IP, visit http://www.designware.com/.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statement

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits and dates of availability of the Synopsys' DDR2 SDRAM memory interface solution. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties in completing the commercial release of the solution, uncertainties attendant to any new Intellectual Property offering, unique elements of customer designs that make use of the memory interface solution difficult or impracticable and certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended July 31, 2006 entitled "Management's Discussion and Analysis of Financial Condition and Results of Operations -- Factors That May Affect Future Results."

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