Synopsys Advances VCS Solution by Adding Assertion IP Library and Native Testbench Support for SystemVerilog

Latest Version of the VCS® Solution Speeds Standards-Based Verification by Unifying SystemVerilog and SystemC™ Languages in a Single Tool

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced it is advancing its VCS® comprehensive RTL verification solution by incorporating a number of new capabilities that enable engineers to find more design bugs faster and achieve up to five times faster verification performance. First, the VCS 2005.06 release includes the new VCS Assertion IP Library, which includes protocol checkers for industry standards such as AMBA™ 2 AHB/APB protocols and PCI® interfaces. Second, the VCS solution extends its customer-proven, high-performance Native Testbench (NTB) technology to incorporate an industry-first, full-featured SystemVerilog testbench solution. Finally, VCS 2005.06 delivers native SystemC language simulation.

"Customers are asking for proven verification technology that combines easy-to-use assertion and verification IP with support for industry standards," said Manoj Gandhi, senior vice president and general manager, Verification Group, Synopsys, Inc. "Synopsys has always been committed to delivering industry standards support in our VCS solution. The latest release now combines our proven, Native Testbench and assertion-based verification technology with SystemVerilog and SystemC languages to deliver higher verification throughput with the flexibility provided by open standards."

VCS Assertion IP Library for Industry-Standard Protocols

The VCS Assertion IP Library contains a set of checkers that can be used with the VCS solution or with Synopsys' Magellan™ hybrid RTL formal analysis tool to verify complex protocols within the design. The VCS Assertion IP Library allows designers to perform functional checks during simulation, identify and report protocol violations, and capture assertion coverage data. Additionally, engineers can use the library with the Magellan tool to prove complex design properties. Combined with the constrained-random stimulus generation and self-checking capabilities of DesignWare® Verification IP, the VCS Assertion IP Library enables design teams to create comprehensive block-level and chip-level verification environments that comply with Synopsys' Reference Verification Methodology guidelines to increase design quality and lower development cost. The VCS Assertion IP can be used with designs created with SystemVerilog, Verilog, VHDL or SystemC languages.

Included as a standard feature with the VCS 2005.06 release, the VCS Assertion IP is provided for the following interface and protocol standards:

-- PCI and PCI-X® 2.0 interface
-- AMBA 2 AHB and APB
-- 802.11a-g
-- AGP
-- SMIA
-- DDR2
-- OCP 2.0
-- LPC

Additional protocol standards are planned to be supported in future releases of the VCS solution, including PCI Express™ interface, USB 2.0 and CoreConnect.

Native Testbench Technology Extended with SystemVerilog Support

The latest version of the VCS solution now supports IEEE P1800 SystemVerilog testbench features natively with its Native Testbench technology. Engineers using the VCS solution can now quickly create highly effective verification environments using SystemVerilog's object-oriented, constrained-random stimulus and functional coverage capabilities. VCS' NTB technology deploys a unique, single-compiler architecture to simultaneously optimize design, testbench, assertions and coverage. This powerful combination delivers up to five times faster verification performance compared to independent testbench and simulation environments.

"Stretch is successfully using VCS' NTB technology to accelerate our verification performance," said Wayne P. Heideman, vice president of Engineering at Stretch, Inc. "Now that the VCS solution includes testbench support for the industry-standard SystemVerilog language, we again expect to advance our verification testbench environment for the S5000 family of software-configurable processors."

In addition to support for SystemVerilog design constructs, assertions and the Direct Programming Interface (DPI), the VCS 2005.06 release now adds native support for the following SystemVerilog testbench features:

-- Automatic static task/functions
-- Clocking block
-- Dynamic and associative arrays
-- Functional coverage
-- Object-oriented programming and encapsulation
-- Program block
-- Queues
-- Random constraints
-- Threading and synchronization
-- Virtual interfaces

Built-In SystemC Language Simulator

VCS 2005.06 includes a native SystemC language simulator with support for flexible co-simulation of mixed-HDL designs and SystemC models. The VCS native SystemC language simulation capability is compliant with the OSCI SystemC language 2.0.1 standard.

Availability

VCS 2005.06 is expected to be available in the third calendar quarter of 2005.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits and date of availability of VCS 2005.06. These statements are based on Synopsys' current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties in completing development of the release, uncertainties attendant to any new product release and the other factors contained in Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended January 31, 2004.

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