Arm and Synopsys to Deliver Industry's First Reference Verification Methodology Based on SystemVerilog

Companies to Publish 'SystemVerilog Verification Methodology Manual,' A 'How-to' Book on Verification Using SystemVerilog

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CAMBRIDGE, England, and MOUNTAIN VIEW, Calif.

ARM (LSE: ARM); (NASDAQ: ARMHY), the industry's leading provider of 16/32-bit embedded RISC processor solutions, and Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced at DATE, Paris, France, that they are jointly developing a reference methodology to define a coverage-driven verification architecture using SystemVerilog, the open, industry-standard language. ARM and Synopsys will publish the methodology in the co-authored "SystemVerilog Verification Methodology Manual (VMM)." The SystemVerilog VMM will provide engineers with architecture guidelines and industry best practices that enable more effective and faster functional verification of complex systems-on-chips (SoCs). It will also provide verification IP developers with a standard verification architecture to foster the development of interoperable verification IP. The SystemVerilog VMM will be on show at the 2004 Design Automation Conference (DAC), in San Diego, Calif.

"ARM is actively working with Synopsys to satisfy our Partners' needs to use SystemVerilog for verification," said John Goodenough, worldwide design methodology manager at ARM. "By teaming with Synopsys on the SystemVerilog VMM, we are addressing the industry need for a proven methodology to implement a coverage-driven verification environment based on an open, industry-standard language."

SystemVerilog Reference Verification Methodology

The methodology described in the SystemVerilog VMM will combine the ARM® expertise in the verification of complex, configurable IP from transaction- level SystemC to timing-critical register-transfer level (RTL) implementation, and Synopsys' strength in delivering an integrated RTL and system verification platform, including tools and verification IP. It will provide a blueprint for a robust, scalable verification architecture based on industry best practices. The methodology will address all aspects of functional verification, including design-for-verification techniques using SystemVerilog Assertions (SVA) for formal analysis and dynamic verification; use of constrained-random stimulus generation techniques; and use of coverage metrics to achieve rapid verification closure. The methodology will also enable verification IP providers to adhere to a consistent and well-documented architecture, enabling end users to easily integrate verification IP from multiple sources.

"The growing adoption of SystemVerilog has created an industry need for a robust verification methodology to enable customers to take advantage of this unified language," said Vassilios Gerousis, Accellera's technical committee chairman. "The methodology developed by the ARM-Synopsys collaboration and documented in the SystemVerilog VMM will accelerate the adoption of SystemVerilog to address the growing verification challenge."

"SystemVerilog provides the first industry opportunity to define a unified methodology that brings together the capabilities of assertions, testbench and functional coverage in a single design and verification language," said Manoj Gandhi, senior vice president and general manager, Synopsys Verification Group. "ARM and Synopsys are combining their strengths to deliver this methodology. Similar to how the Reuse Methodology Manual (RMM) made design reuse a reality, the SystemVerilog VMM will foster verification best practices and deliver the power of SystemVerilog throughout the industry."

SystemVerilog Verification Methodology Manual

The manual will describe SystemVerilog language features relevant to functional verification as well as document a robust, reusable verification methodology to enable faster and more effective design verification. The manual will deliver a specification of a standard set of libraries for assertions and commonly used verification functions, such as stimulus generation, simulation control and coverage analysis to help implement the recommended methodology. The SystemVerilog VMM will be based on hundreds of years of collective verification and IP experience from ARM and Synopsys, including experience from experts, such as Janick Bergeron, moderator of Verification Guild and a principal Synopsys R&D engineer; Phil Moorby, creator of Verilog HDL and a Synopsys scientist; Peter Flake, a Synopsys scientist; and John Goodenough, ARM worldwide design methodology manager. By following the guidelines and techniques described in the SystemVerilog VMM, engineers will be able to take advantage of the architecture used by experts.

"Every verification project requires a detailed methodology that aims for first-time success," said Janick

Bergeron, moderator of Verification Guild and a principal R&D engineer at Synopsys, Inc. "The SystemVerilog VMM will teach engineers how to create a single, reusable verification environment that can be used to verify transaction-level models written in SystemC as well as the RTL implementation of the design. The methodology documented in the SystemVerilog VMM will reduce the amount of code needed to write and maintain tests, and enable extensive re-use within and between projects."

"We welcome the ARM-Synopsys collaboration to deliver a robust verification architecture based on SystemVerilog," said Glen Henshaw, director, Ottawa Technology Center at Altera. "Our IP product development cycle is highly compressed, putting significant pressure on functional verification schedules and effectiveness. The SystemVerilog VMM's documented verification architecture will enable us to deploy sophisticated techniques and achieve our product development goals with lower risk."

Availability

The SystemVerilog Verification Methodology Manual will be on show in June at DAC 2004.

About ARM

ARM is the industry's leading provider of 16/32-bit embedded RISC microprocessor solutions. The company licenses its high-performance, low-cost, power-efficient RISC processors, peripherals and system-chip designs to leading international electronics companies. ARM also provides comprehensive support required in developing a complete system. ARM's microprocessor cores are rapidly becoming the volume RISC standard in such markets as portable communications, hand-held computing, multimedia digital consumer and embedded solutions. More information on ARM is available at http://www.arm.com/.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading IC design and verification platforms to the global electronics market, enabling the development of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Forward Looking Statements

This press release contains forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected date of availability of the SystemVerilog Verification Methodology Manual and the expected benefits of the methodologies expected to be described therein. These statements are based on ARM's and Synopsys' current expectations and beliefs. Actual results could differ materially from the results implied by these statements as a result of unforeseen difficulties in completing the description of the methodology and uncertainties attendant to development of any new IC design or verification methodology, as well as factors described in the reports filed by ARM and Synopsys with the United States Securities and Exchange Commission.

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