Synopsys and UMC Enhance 90-nm Reference Flow With Advanced Low Power and Design for Test

Synopsys' Galaxy Design Platform Validated With Multi-Vdd Capability for UMC's 90-nm Process

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, and UMC (NYSE: UMC)(TSE: 2303), a world-leading semiconductor foundry, today announced that the two companies have collaborated to add new capabilities to the reference design flow based on Synopsys' Galaxy™ Design Platform for UMC's 90-nanometer (nm) process.

The advanced low-power design flow, initially introduced in November 2005 (see http://www.umc.com/english/news/2007/20070109.asp), now includes an automated multiple voltage (multi-Vdd) capability that can reduce dynamic power and leakage power dissipation significantly. New design-for-test (DFT) capabilities have also been added to the flow, and existing design for manufacturing (DFM) capabilities were validated with UMC's libraries. These additions help IC companies reduce risk and achieve predictable success for complex low-power designs.

The RTL-to-GDSII reference flow helps designers address multi-voltage design challenges such as dynamic power and leakage, which are especially important in 90-nm designs. The reference flow features level shifter insertion, placement, optimization and verification, as well as voltage area (VA) creation and VA-aware physical optimization, clock-tree synthesis and routing. The timing closure flow includes signal integrity (SI) prevention, repair and sign-off with multi-voltage physical verification. In addition, the flow includes full-chip power analysis and power network analysis to ensure the power integrity of the design. Synopsys' DFT MAX scan compression automation solution is now included in the reference flow to enable higher test quality and to reduce tester application time. The 90-nm reference flow also features Synopsys' DFM technology for redundant via insertion, via- farm/via-array rules and timing-driven metal fill.

To validate the effectiveness of the reference flow, design consultants from Synopsys' Professional Services collaborated with UMC engineers to design a test chip with an open source 32-bit RISC microprocessor core. The test chip, which was validated with UMC's library, was partitioned into multiple voltage regions and implemented using the advanced low-power reference flow. The core consisted of a SPARC-V8 compliant 32-bit RISC CPU, industry standard AMBA system buses, 10/100 Ethernet MAC and standard PCI interfaces. The chip is highly configurable and expandable for additional digital and/or analog/mixed-signal intellectual property (IP) modules.

"Our successful partnership with Synopsys gives our customers access to a validated 90nm reference flow that reduces risk and speeds time to market," said Ken Liou, director of the IP and Design Support division at UMC. "Our continued collaboration with Synopsys Professional Services ensures that the performance and capabilities of the Galaxy Design Platform will work smoothly in UMC's most advanced process flows."

"Synopsys works closely with world-class foundries like UMC to ensure that our mutual customers have access to a proven flow that targets low power and DFM requirements," said Rich Goldman, vice president of Strategic Market Development at Synopsys. "This collaboration helps ensure that Synopsys' Galaxy Design Platform offers UMC customers a complete, reliable RTL-to-GDSII design flow. We will continue to work with UMC to address future challenges as we move to even deeper submicron processes."

Availability

The UMC/Synopsys reference design flow is available today and can be accessed from UMC's website at https://my.umc.com/ . The reference design flow was jointly developed by UMC and Synopsys Professional Services.

About UMC

UMC is a leading global semiconductor foundry that manufactures advanced process ICs for applications spanning every major sector of the semiconductor industry. UMC delivers cutting-edge foundry technologies that enable sophisticated system-on-chip (SoC) designs, including 90-nm copper, 0.13 micron copper, embedded DRAM, and mixed signal/RFCMOS. UMC is also a leader in 300mm manufacturing. In addition, UMC is a leader in 300mm manufacturing with strategically located 300mm fabs to serve our global customer base: Fab 12A in Taiwan and Fab 12i in Singapore. UMC employs over 12,000 people worldwide and has offices in Taiwan, Japan, Singapore, Europe, and the United States. UMC can be found on the web at

http://www.umc.com/ .

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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