Toshiba Adopts Synopsys IC Compiler for Use in Its SoC Research and Development Center

IC Compiler Delivers 10 Percent Higher Speed With Faster Time-To-Results

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.

Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Toshiba Corporation, a leader in information and communications systems, consumer products and power systems, is adopting Synopsys IC Compiler for use in its System-on-chip (SoC) Research and Development Center. IC Compiler was launched at Synopsys' Users Group meeting in March 2005 with live presentations from four early adopters. A centerpiece of Synopsys Galaxy™ Design Platform, IC Compiler is the next-generation physical implementation system. It incorporates extended physical synthesis (XPS) technology extending physical synthesis to full place-and-route, signoff-driven design, and yield-driven optimizations.

"We think IC Compiler is the next breakthrough technology from Synopsys after its Physical Compiler® product," said Masataka Matsui, senior manager, Digital Media SoC Department, SoC R&D Center, Toshiba Corporation Semiconductor Company. "With IC Compiler we were able to achieve 10 percent higher clock speed and substantially improved signoff correlation, resulting in faster timing closure. Encouraged by these results, we have decided to use IC Compiler for our next 90-nanometer SoC."

Driven by their need for a physical implementation solution that delivers comprehensive timing, area, power, signal integrity, and yield technology with faster turnaround time, Toshiba's SoC R&D Center is collaborating closely with Synopsys on IC Compiler. They evaluated IC Compiler on a previous 90-nanometer design running at 400 MHz. IC Compiler provided a 10 percent improvement in clock speed through its XPS technology, tight correlation to signoff, and easy fit into Toshiba's existing flow. As a result of this successful evaluation, Toshiba's SoC R&D Center is adopting IC Compiler for use on a 90-nanometer SoC using Media embedded Processor (MeP) modules.

"Toshiba is a world leader in high technology, and their chips are on the forefront of leading-edge design. The XPS technology in IC Compiler was engineered to address these very needs," said Antun Domic, senior vice president and general manager, Synopsys. "We are very pleased to see Toshiba join the ranks of early adopters who are actively using IC Compiler to gain a competitive edge."

About IC Compiler

IC Compiler provides superior results by harnessing the best of Synopsys core technologies in synthesis, timing, placement, routing, lithography and signoff, coupled with new innovations in physical design. Current generation solutions integrate physical design steps into a single executable, but have limited horizon because placement, clock tree and routing are separate, disjoint steps. Yield optimizations and timing signoff are also separate. IC Compiler unifies physical design through innovations in optimizations, yield enhancement and timing/SI signoff. IC Compiler extends physical synthesis to full place and route using XPS technology, breaking down the walls between placement, clock tree and routing in current generation solutions.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

NOTE: Synopsys, and Physical Compiler are registered trademarks of Synopsys, Inc., Galaxy is a trademark of Synopsys. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contacts:
Nancy Renzullo
Synopsys, Inc.
(650) 584-1669
renzullo@synopsys.com

Sarah Seifert
Edelman
(650) 429-2776
Sarah.seifert@edelman.com

SOURCE: Synopsys, Inc.

CONTACT: Nancy Renzullo of Synopsys, Inc., +1-650-584-1669, or renzullo@synopsys.com; or Sarah Seifert of Edelman, +1-650-429-2776, or Sarah.seifert@edelman.com, for Synopsys

Web site: http://www.synopsys.com/