

Synopsys' Proteus Optical Proximity Correction Software Delivers Near Linear Performance Increase Using 1000 Intel® Xeon™ Processors

Scalable Distributed Processing Significantly Reduces OPC Processing Time

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Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced significantly improved performance of its Proteus™ optical proximity correction (OPC) software through its distributed processing capability on the Intel® Xeon™ architecture. With demonstrated near-linear scalability when distributed on more than 1000 Intel Xeon processors, Proteus can now reduce the time to obtain OPC results from days to hours on advanced 90-nanometer (nm) and 65nm integrated circuits (ICs). Synopsys' leading semiconductor customers have taped out complex designs containing over 500 million transistors with Proteus on thousands of Intel Xeon-based compute servers.

"We are pleased to see leading EDA applications like Proteus optimized for Intel® Architecture based systems to drive significant improvements in silicon design," said Guru Bhatia, IT Engineering Computing Director, Intel Corporation. "Highly scalable large compute environments based on Intel Xeon processors offer higher performance and faster throughput required to design complex silicon products at a lower cost.

"Proteus has become critical to ensure the manufacturability of the most advanced semiconductor designs," said Sandeep Khanna, vice president of the design for manufacturing group at Synopsys. "The ability to achieve accurate OPC results on a complete design in less than twelve hours is crucial for most of our customers. Proteus' scalable distributed processing, combined with Intel Xeon processors, delivers on this goal."

Synopsys will offer live demonstrations of Proteus' scalability on 80 Intel Xeon processors at 3.06 GHz, in a rack at SPIE's Microlithography 2004 Conference in booth #820 at the Santa Clara Convention Center on February 24 and 25, 2004. For more information about Synopsys' participation in the conference please visit:

<http://www.synopsys.com/news/events/conference04/microlithography04/micro.html> .

About Synopsys DFM

Synopsys offers the industry's most comprehensive RTL-to-Mask design-for-manufacturing (DFM) solution. Its DFM product family addresses critical yield and manufacturability issues with its software products: Proteus™ mask synthesis, CATS™ mask data preparation, SiVL® lithography verification, iVirtual Stepper™ mask defect positioning and Taurus™ TCAD. Synopsys leverages this expertise in its industry-leading Galaxy™ Design Platform implementation solution in order to help ensure that designs at 90nm and smaller geometries will meet key manufacturing requirements. Synopsys' DFM product family is the solution-of-choice at leading semiconductor manufacturers worldwide. Eighty percent of all sub-180nm microprocessors and fifty percent of all DRAMs produced use Proteus, and more than seventy percent of all photomasks produced use CATS.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms to the global electronics market, enabling the development of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and is located in more than 60 offices throughout North America, Europe, Japan and Asia. Visit Synopsys online at <http://www.synopsys.com/> .

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SOURCE: Synopsys, Inc.

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