TSMC Reference Flow 7.0 Incorporates Synopsys' IC Compiler

Reference Flow 7.0 Incorporates Latest Technologies for Low Power and Yield Optimization to Address 65-nanometer Design Challenges

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, and Taiwan Semiconductor Manufacturing Company (NYSE: TSM) -- the world largest semiconductor foundry, today announced Synopsys' Galaxy™ design and DFM platforms support in TSMC's Reference Flow 7.0. The Reference Flow 7.0 includes Synopsys' IC Compiler next-generation physical implementation to provide new low-power and yield capabilities that address 65-nanometer design challenges. This collaborative effort between the two companies brings together advanced semiconductor design and manufacturing to achieve optimum IC performance, power, and yield with higher predictability.

TSMC's Reference Flow 7.0 utilizes key capabilities of Synopsys' Galaxy design platform to address low-power and yield requirements, including:

-- Concurrent multi-corner/multi-mode optimization for multi-voltage designs
-- Chemical mechanical polishing (CMP)-aware model-based metal fill for optimal results in metal thickness

"As customers move their designs into 65-nanometer processes, power management and design for manufacturing become as important as traditional timing and signal integrity challenges," said Ed Wan, senior director of design service marketing at TSMC. "Synopsys' newest design and manufacturing capabilities address the key requirements of TSMC's Reference Flow 7.0 to maximize the benefits of our advanced technology for 65-nanometer design."

"TSMC and Synopsys continually evaluate and address the needs of our designers with enhancements to the Reference Flow," said John Chilton, senior vice president and general manager of Synopsys' Solutions Group. "Our ongoing collaborative efforts help ensure that Synopsys' low power-optimization, statistical analysis and advanced yield technologies provide optimum silicon performance with high predictability."

Power Optimization and Analysis

The TSMC Reference Flow 7.0 includes new low-power design capabilities within Synopsys' Galaxy design platform, including power domain specification and verification at the RTL level, concurrent multi-corner/multi-mode optimization for multi-voltage designs, coarse-grain multi-threshold CMOS (MTCMOS) logic for leakage mitigation, and dynamic voltage-drop analysis considering MTCMOS rush currents. Synopsys' existing production-proven low-power design methodologies such as clock gating, power network synthesis, power-aware placement, low-power clock-tree synthesis, multi-threshold leakage power optimization, and static/dynamic voltage-drop analysis are also included in the Reference Flow 7.0.

Design For Manufacturing (DFM)

Reference Flow 7.0 includes new capabilities that enhance yield during design, including implementation support for 65-nanometer design rules, Critical Area Analysis (CAA), and CMP simulation and metal fill.

About TSMC Reference Flow 7.0 Support

Reference Flow 7.0 incorporates a complete Synopsys-based RTL-to-GDSII solution utilizing the Galaxy Design Platform for RTL synthesis, physical implementation and sign-off, and the Discovery™ Verification Platform with VCS® and HSPICE® for RTL verification and circuit simulation. As an integral part of the reference flow, extensive Galaxy support includes Design Compiler® logic synthesis solution, Power Compiler™ multi-voltage power management solution, Leda RTL Checker, DFT MAX 1-pass test synthesis solution, Jupiter-XT™ physical planning solution, IC Compiler physical implementation solutions, PrimeTime and PrimeTime SI static timing and signal integrity sign-off solutions, PrimeRail power network sign-off solution, PrimePower and PrimeTime PX full-chip power analysis solution, Star-RCXT extraction solution, Hercules™ PVS physical verification solution, and TetraMAX® automatic test generation (ATPG) solution. In addition, Synopsys Professional Services provides expertise in chip implementation and flow deployment services with Reference Flow 7.0.

About TSMC

TSMC is the world's largest dedicated semiconductor foundry, providing industry's leading process technology and the foundry industry's largest portfolio of process-proven library, IP, design tools and reference flows. The company operates two advanced twelve-inch wafer fabs, five eight-inch fabs and one six-inch wafer fab. TSMC also has substantial capacity commitments at its wholly owned subsidiaries, WaferTech and TSMC (Shanghai), and its joint venture fab, SSMC. TSMC is the first foundry to provide 65nm production capabilities. Its corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please see http://www.tsmc.com/ .

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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