Synopsys Reduces AMBA Bus-Based SoC Design Time With DesignWare Library

New DesignWare AMBA Connect Automates IP Selection, Configuration, Assembly, Simulation and Synthesis

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Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced DesignWare® AMBA™ Connect, a new feature in its DesignWare Library that dramatically reduces design time, effort and risk for AMBA bus-based designs. This feature uses Synopsys' coreAssembler tool to automate AMBA design knowledge and to replace manual, time-consuming and error-prone tasks of subsystem IP assembly, implementation and verification. More than 25,000 DesignWare Library users now have access to coreAssembler technology and this packaged AMBA knowledge for no additional charge.

DesignWare AMBA Connect automates IP selection, configuration, assembly, simulation and synthesis for AMBA bus-based designs. Based on a designer's chosen configuration, DesignWare AMBA Connect generates an appropriately configured memory map, RTL modules, fully wired top-level netlist and, testbench infrastructure with stimulus to validate the interconnections using and DesignWare AMBA Verification IP. DesignWare AMBA Connect supports both the full AMBA 2.0 functionality as well as AHB-Lite and automatically generates single or multi-layer AMBA subsystems, including the necessary bus and bridge structures.

"DesignWare AMBA Connect is the only comprehensive solution to offer knowledge-based assembly of implementation and verification IP for AMBA-based subsystems," said Guri Stark, vice president of Marketing, Synopsys Solutions Group. "We continue to enhance our extensive DesignWare Library IP portfolio, and the addition of coreAssembler technology, can enable designers to create AMBA bus-based designs in hours rather than weeks."

Pricing and Availability

DesignWare AMBA Connect is included in the DesignWare Library and will be available as part of the Synopsys 2004.06 release in June. DesignWare Library licensees will have access to AMBA Connect for no additional cost. DesignWare Library is available on a subscription or perpetual license basis. Synopsys' coreAssembler tool is included in DesignWare Library at no extra charge to assemble DesignWare IP. It is available for a separate charge for non-DesignWare IP.

About DesignWare Library

The Synopsys DesignWare Library reduces design risk by providing high quality, silicon-proven IP for ASIC, SoC, and FPGA designs. With a comprehensive portfolio of pre-designed implementation IP, verification IP, and foundry libraries, the DesignWare Library improves productivity for a faster time to market and helps users achieve the best quality-of-results for datapath intensive designs. The DesignWare Library portfolio includes foundry libraries, verification IP, AMBA bus IP and peripherals, memories, building block IP and microcontrollers. All are available under one license with no additional costs, per use fees, or royalties.

For a complete directory of Synopsys' available IP visit: www.synopsys.com/ipdirectory For more information on DesignWare IP, visit: www.designware.com or call 1-877-4BEST-IP

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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