Synopsys' DFM Environment Selected by Texas Instruments for Design and Process Development for the 65-Nanometer Node and Beyond

Synopsys' PSM, Hercules PVS, Proteus OPC and TCAD Offer FastDFM Flow Turnaround Time

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software today announced that Texas Instruments (TI) has adopted the Synopsys Design-for-Manufacturing (DFM) environment for its 65 nanometer (nm) and beyond designs. TI extended its use of Synopsys' Alternating Aperture Phase Shift Mask (AA-PSM) and Proteus Optical Proximity Correction (OPC) technologies for the 65-nm node. TI also has adopted Hercules™ Physical Verification Suite (PVS) and FLOOPS process and DESSIS device simulation tools as the Technology CAD (TCAD) simulation platform for its future 45-nm process. This development demonstrates how the Synopsys environment addresses key 45-nm challenges, including fast turnaround time for the manufacturing flow, from design to tapeout.

Several high-performance IC manufacturers already use Synopsys' AA-PSM technology in production. This technology has been employed to fabricate transistors as small as 9 nm -- the world's smallest transistors manufactured with 248 nm lithography equipment. At 65-nm and 45-nm nodes, having strong control over the lithography process is a critical component in meeting targeted yield goals.

"Synopsys phase-shift technology allows us to tightly control lithography resolution and enhance yields on our high-performance chips," said Mark Mason, resolution enhancement technology manager, Texas Instruments. "Synopsys' mask synthesis solutions offer the critical dimension accuracy and near-linear scalability that we require to meet the complex data processing needs for our advanced 65- and 45-nanometer technology."

As process geometries continue to shrink, the critical links between DFM tools and the ability to efficiently optimize the application of OPC play an increasingly critical role in accelerating time-to-yield. In addition, OPC at smaller geometries requires significantly more processing time. The architecture of Synopsys' Proteus OPC tool provides near-linear scalability, when using clusters of inexpensive Linux-based central processing units (CPUs) that allow customers to reduce turn-around-time.

Hercules PVS delivers the features and programmability required to handle complex 45-nm DRC rules along with the distributed processing technology, which scales well over many CPUs. Hercules PVS is the engine for a number of manufacturing applications for other Synopsys DFM products such as PSM and SiVL® Lithography Rule Checking.

"As process geometries continue to shrink, it is very important that TI have a high performance, flexible physical verification engine that is well integrated with other manufacturing products along the flow," said Mike Fazeli, manager of EDA strategies, Texas Instruments.

For development of high-performance transistors at 45-nm and below, TI has selected Synopsys' FLOOPS and DESSIS as the TCAD simulation platform. FLOOPS and DESSIS, the technologies that the new Synopsys TCAD platform is based on, include both 2D and 3D simulation capabilities that address the increasing demand of physical modeling in each new technology node.

"State-of-the-art TCAD is vitally important to TI's leadership in technology," said Dennis Buss, vice president of silicon technology development, Texas Instruments. "After careful evaluation, we have selected FLOOPS and DESSIS for the 45 nanometer technology node. We believe these tools will enable us to maintain our leadership into 45 nanometer CMOS. We look forward to a continuing relationship with Synopsys to maintain FLOOPS and DESSIS at the forefront of technology."

TCAD tools are a critical part of the overall DFM solution as they precisely simulate advanced semiconductor processes and devices down to the atomic level before they are put into production. The use of TCAD during process development helps reduce cost and time to optimization and characterize new process and device technologies.

"TI has utilized Synopsys' TCAD technology to develop succeeding generations of advanced process technology ahead of the competition," said Raul Camposano, general manager of the Silicon Engineering Group at Synopsys. "Synopsys' 'DFM aware' environment enables customers like TI to achieve high QoR through four segments of the process: design, verification, mask optimization and process tuning. Our expanded relationship with TI as a manufacturing company helps further the development of leading-edge, innovative semiconductor technologies. Both companies are strongly aligned to address and solve key challenges for 65 nanometer and beyond."

About Synopsys DFM

Synopsys offers the industry's most comprehensive RTL-to-Mask DFM solution. Its DFM product family addresses critical yield and manufacturability issues with its Hercules Physical Verification Suite (PVS), Synopsys PSM, Proteus mask synthesis, CATS® mask data preparation, SiVL lithography verification, i-Virtual Stepper™ mask defect dispositioning, and physics-based TCAD suite of simulation products. Synopsys leverages this expertise throughout its industry-leading Galaxy™ Design Platform implementation solution to help ensure that designs at 90 nanometers (nm) and smaller geometries will meet key manufacturing requirements. Synopsys' DFM product family is the solution-of-choice for yield sensitive, high-value chips, worldwide. Eighty percent of all sub-180-nm microprocessors, 60 percent of all sub-180-nm DRAMs, 80 percent of all sub-180-nm FPGA and graphics chips, 70 percent of all sub-180-nm cellular baseband chips produced use Proteus, and more than 80 percent of all photomasks produced use CATS.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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