SANYO Improves Test Quality With the Adoption of DFT MAX

Simple Implementation and Predictable Results Were Key Drivers in Selection

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that SANYO Semiconductor Co., Ltd., a leading supplier of consumer electronics products, has adopted the Synopsys DFT MAX scan compression automation solution to further increase the test quality of its digital designs. Using DFT MAX, SANYO engineers decreased test data volume by more than 90 percent, enabling them to achieve their high-quality test goals in less time. DFT MAX takes advantage of physical-aware links within the Synopsys Galaxy™ Design Platform, enabling designers to avoid costly iterations and achieve rapid design closure.

SANYO's engineers required the flexibility to generate many more patterns, if needed, to reach the highest-quality at-speed testing of their large-scale integration (LSI) circuits. However, they realized increasing the quality would lead to a larger volume of test data without an effective way to compress the data to fit within tester memory constraints.

"We found that we could meet our high-quality goals by adding DFT MAX to our Galaxy Design Platform flows," said Hiroyuki Oike, general manager of SANYO's System Solutions Business division. "After thoroughly evaluating DFT MAX to implement on-chip compression, we decided to adopt it for all our future LSI designs."

SANYO designers wanted a solution that would not only meet their compression goals, but would also be as easy to implement as traditional scan. DFT MAX's ease-of-use, combined with its seamless integration with other flows in the Galaxy Design Platform, allowed SANYO designers to quickly migrate to DFT MAX and achieve greater than 90 percent digital test data volume reduction for two LSIs: a four-million-gate communication chip and a two-million-gate digital imaging chip. For each of these designs, DFT MAX needed just 0.1 percent and 0.2 percent additional gates for compression.

"We adopted DFT MAX because we were able to improve the quality for our complex designs and achieve this with less test data volume and less test time," said Yuji Shiine, digital design section manager in SANYO's Design Engineering Department. "And migrating to DFT MAX was easy because it required little effort to integrate it into our existing DFT Compiler™ flows. As a result, we are going to use DFT MAX with the other solutions in Synopsys' Galaxy Design Platform in our effort to continually improve the quality and technical differentiation of our products."

"SANYO's adoption of DFT MAX further validates the need for a compression solution that is simple to implement and does not impact the physical implementation of the chip," said Graham Etchells, director of Test Marketing, Synopsys Implementation Group. "Our customers are seeing immediate and substantial return-on-investment using DFT MAX because the tool is easy to use and achieves highly predictable compression results. Also, since DFT MAX takes advantage of physical-aware links within the Galaxy Design Platform, it has negligible timing and area impact on the physical implementation of the chip, enabling rapid design closure. In contrast, compression architectures that require sequential logic can require many more iterations to converge on timing and take much longer to achieve design closure."

About SANYO

SANYO Electric Co., Ltd. is a leading provider of Environment and Energy-related products and services with over $20 billion in sales per year. SANYO's businesses cover a broad range of both consumer and commercial products such as commercial equipment, rechargeable batteries, AV/information and communications equipment, home appliances, electronic devices, and others. SANYO is committed to providing cutting-edge solutions for a sustainable world by weaving together its numerous proprietary technologies. For further information, please visit SANYO's website at http://www.global-sanyo.com/ .

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit

Synopsys online at www.synopsys.com .

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, or sgulizia@synopsys.com

Web site: http://www.synopsys.com/
http://www.global-sanyo.com/