Altera Collaborates With Synopsys on Hardcopy Structured ASICs

Industry Leaders Team Up To Provide Unified Solution for FPGAs, Structured ASICs and ASICs

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Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, and Altera Corporation (NASDAQ: ALTR), the world's pioneer in system-on-a-programmable-chip (SOPC) solutions, today announced an agreement for the establishment of Synopsys Professional Services resources to support the HardCopy® design center. This agreement is driven by the rapidly growing demand for HardCopy devices in the marketplace. The collaboration will accelerate HardCopy device implementation by establishing an advanced and optimized back-end design flow and provide access to expert physical design resources that will complement Altera's existing HardCopy design center. Additionally, designers can now use Synopsys' Galaxy™ Design Platform front-end flow to design their Stratix FPGA.

The agreement builds on work already in progress for the development of a new timing-driven HardCopy back-end design flow based on Synopsys' leading Galaxy Design Platform and optimized for Altera's FPGA-to-HardCopy migrations. The flow will be used by Altera and Synopsys to further optimize the chip performance and reduce the turn-around-time of HardCopy implementations. Once a customer's design is verified in a Stratix® FPGA, the Altera HardCopy Design Center performs the necessary back-end design services required to build production masks. Based on Synopsys Professional Services' many years of experience in implementing leading-edge FPGA and ASIC designs, Altera will utilize Synopsys as complementary design resources to support these implementation efforts. Services performed will include place-and-route, design rules checking, formal verification, and the generation of the final GDSII artwork. Using the Synopsys Galaxy flow helps Altera deliver fast and predictable turnaround times to HardCopy users.

Customers can now target Altera Stratix FPGAs and HardCopy devices with the front-end Galaxy design platform, which includes Design Compiler® (DC) FPGA, DesignWare ®, Formality®, and PrimeTime®. DC FPGA allows designers to design once at the RTL for the FPGA or HardCopy structured ASIC. Designers can then reuse their source description, synthesis scripts, constraint files and DesignWare IP to migrate the design from FPGA to a HardCopy Structured ASIC or a standard cell ASIC.

Altera's use of Synopsys' Galaxy solution provides for fast turnaround times for the seamless migration of Stratix FPGAs to HardCopy Structured ASICs. The HardCopy design flow utilizes Star-RCXT™ for parasitic extraction with PrimeTime for static timing analysis, PrimeTime SI for signal integrity analysis, DFT Compiler™ for the test circuit synthesis in combination with TetraMAX™ for the test pattern generation, and Astro™ for the HardCopy device place and route.

"Using Synopsys' market-proven design tools throughout the design cycle allows our customers to get their designs into our high-performance devices with as little risk as possible," said John Daane, CEO of Altera Corporation. "Reducing risk is key to customer success. "With the help of the world's leading EDA company, more customers can leverage the unique capabilities offered in HardCopy structured ASICs to lower their costs and bring their designs to market faster."

"Altera's high-performance programmable devices are surpassing today's median ASICs in terms of complexity. These kinds of design challenges call for ASIC-strength solutions and methodologies," said Aart de Geus, chairman and CEO at Synopsys. "By using Synopsys technology and design services that are proven on ASICs, but tailored to programmable logic design, engineers can design once and target their design to an FPGA, HardCopy structured ASIC or an ASIC using the same convergent, low risk flow."

About HardCopy Stratix Devices

Altera's HardCopy Stratix devices are the industry's most unique structured ASICs, offering a seamless migration path from an FPGA prototype to a low-cost mask-programmed device. Accessible through Altera's Quartus® II software, HardCopy devices deliver ASIC-level performance, price, and features that customers can take to production risk-free. HardCopy Stratix devices have the same features as the successful Stratix FPGAs and offer an average 50 percent performance increase. HardCopy devices also consume up to 40 percent less power compared to the equivalent Stratix FPGAs. Altera's HardCopy Stratix devices are ideal for high-performance, high-volume applications in the storage, networking, wireless communication, consumer electronics, and industrial markets. For more information about HardCopy Stratix devices, please visit www.altera.com/hardcopystratix.

About Altera

Altera Corporation is the world's pioneer in system-on-a-programmable-chip (SOPC) solutions. Combining programmable logic technology with software tools, intellectual property, and technical services, Altera provides high-value programmable solutions to approximately 14,000 customers worldwide. More information is available at www.altera.com.

About Synopsys

Synopsys, Inc. is the world leader in EDA software for semiconductor design. The Company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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SOURCE: Synopsys, Inc.

CONTACT: Bruce Fienberg of Altera Corp., +1-408-544-6397, or newsroom@altera.com; or Heather Kettmann of Synopsys, Inc., +1-650-584-4723, or kettmann@synopsys.com; or Sarah Seifert of Edelman, +1-650-429-2776, or sarah.seifert@edelman.com, for Synopsys

Web site: http://www.synopsys.com/