# Synopsys' Hercules Physical Verification Suite Delivers Near Linear Performance Increase on More Than Fifty 64-Bit Intel® Xeon™ Processors

Scalable Distributed Processing Reduces Physical Verification Processing Time from Days to Hours

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced the availability of a new scalable distributed processing technology that delivers an order of magnitude speedup over current production physical verification solutions. Using parallel processing that distributes the input job over several processors, the technology significantly reduces the physical verification processing time from days to hours for advanced 65-nanometer (nm) and 45-nm integrated circuits. The new distributed processing (DP) technology will be included in Synopsys' Hercules™ physical verification (PV) solution, which has already been delivering the fastest foundry sign-off design rule checking (DRC) for 90 nm and above with near-linear scalability up to 12 CPUs.

The technology is being demonstrated in Intel Corporation's booth at DAC 2005 with Hercules reducing the runtime of a customer layout from 43 hours down to one hour and 48 minutes with Intel® architecture-based processors. A Hewlett-Packard rack with 64-bit Intel® Xeon™ processors is used to demonstrate the speedup.

"It's gratifying to see the significant improvements that can be achieved by optimizing leading EDA solutions like Hercules for Intel architecture-based systems," said Guru Bhatia, IT engineering computing director at Intel Corporation. "Highly scalable, large compute environments based on 64-bit Intel Xeon processors offer the performance and throughput required to design complex silicon products at a lower cost."

"Hercules PVS, a proven technology with thousands of production tape-outs, offers high performance compared to other industry EDA solutions and is the tool of choice for the world's largest semiconductor companies," said Raul Camposano, general manager of the Silicon Engineering Group at Synopsys. "Some of Hercules' customers are already qualifying this solution for 45-nanometer flows. The ability to achieve production sign-off on complex designs in only few hours is a huge time and cost savings. Only Hercules offers such a massive scalable distributed processing technology, and when combined with 64-bit Intel Xeon processors, it delivers superior performance."

Pricing and Availability

The Hercules PVS DP capability is expected to be in LCA availability in December 2005. List price for a full technology subscription license of Hercules for one year is $189,000.

About Synopsys DFM

Synopsys offers the industry's most comprehensive RTL-to-Mask DFM solution. Its DFM product family addresses critical yield and manufacturability issues with its Hercules Physical Verification Suite (PVS), Synopsys PSM, Proteus mask synthesis, CATS® mask data preparation, SiVL® lithography verification, i-Virtual Stepper™ mask defect dispositioning, and physics-based TCAD suite of simulation products. Synopsys leverages this expertise throughout its industry-leading Galaxy™ Design Platform implementation solution to help ensure that designs at 90 nanometers and smaller geometries will meet key manufacturing requirements. Synopsys' DFM product family is the solution-of-choice for yield sensitive, high-value chips, worldwide. Eighty percent of all sub-180-nm microprocessors, 60 percent of all sub-180-nm DRAMs, 80 percent of all sub-180-nm FPGA and graphics chips, 70 percent of all sub-180-nm cellular baseband chips produced use Proteus, and more than 80 percent of all photomasks produced use CATS.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

Forward Looking Statements

This press release contains forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits and date of availability of the Hercules PVS DP technology. These statements are based on Synopsys' current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties in releasing the this technology commercially, uncertainties attendant to any new product or technology release and the other factors contained in Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended April 30, 2005.



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