CEVA, Inc. Leverages Synopsys Galaxy and Discovery Platforms for Tape Out of Advanced Mixed-signal, DSP and High Speed Serial Interface Chips

Synopsys' Complete RTL to Silicon Flow Was Key to Designing Complex Mixed-Signal ASICs

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that CEVA, Inc., a leading licensor of digital signal processors (DSP) cores and communications solutions to the semiconductor industry, has taped out its next-generation high-speed serial interface chips and the CEVA-Teak™ DSP using Synopsys' Galaxy™ and Discovery™ platforms.

The CEVA design team cited Synopsys' convergent flow consisting of the following toolset as the reason for their success: Physical Compiler® and Astro™ products for increased capacity, PrimeTime® SI tool for signal integrity, Power Compiler products for power management, and VCS® and NanoSim® software for mixed-signal chip sign-off. The correlation of these tools was key to implementing their complex mixed-signal designs.

CEVA, a leading IP licensing company, uses the world's leading fabrication facilities to harden and prove its designs in silicon. The company chose the Synopsys Galaxy and Discovery solutions to meet the challenges it faced when designing chips for 130-nanometer (nm) processes and below.

"We relied on Synopsys' routing and placement solutions for our 130 nanometer chips, with an eye toward future designs of 3Gbps serial interfaces that we expect to develop in a 90 nanometer process," said John Ryan, vice president of Communications and Navigation at CEVA. "Synopsys offered solutions that were both technically advanced and cost efficient for our future low-power and mixed-signal designs. We look forward to continued success using Synopsys platforms to produce our advanced mixed-signal and communications devices."

"We've enjoyed working closely with an industry leader like CEVA to produce cutting-edge mixed-signal ASICs," said Antun Domic, senior vice president and general manager, Implementation Group at Synopsys. "CEVA relied on our design and verification solutions, especially the Physical Compiler and Astro tools, to bring their designs to tapeout. It was gratifying to see that our flows were able to give CEVA engineers the solutions they needed to complete their designs."

About CEVA

Headquartered in San Jose, California, CEVA is the leading licensor of DSP cores and communications solutions to the semiconductor industry. CEVA markets a portfolio of DSP IPs in three integrated areas: CEVA DSPs, CEVA System Platforms and CEVA Applications, all supported by CEVA Services. CEVA's technology has been embedded in over 70 million devices year-to-date 2004. CEVA was created through the merger of the DSP licensing division of DSP Group and Parthus Technologies. For more information visit www.ceva-dsp.com.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

NOTE: Synopsys, Physical Compiler, NanoSim, PrimeTime and VCS are registered trademarks of Synopsys, Inc. Astro, Discovery and Galaxy are trademarks of Synopsys. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

SOURCE: Synopsys, Inc.

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