S3 Adopts Synopsys' VCS Verification Solution and the Verification Methodology Manual for SystemVerilog

Industry-Standard SystemVerilog Enables Advanced Verification of Complex VHDL Designs

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Dublin-based Silicon & Software Systems Ltd. (S3), a leading provider of design and consulting services for integrated circuits and embedded software, is supporting the Synopsys VCS® comprehensive RTL verification solution and the Verification Methodology Manual (VMM) for SystemVerilog. S3 will use the VCS solution and the VMM for SystemVerilog to develop products for a wide variety of wireless, consumer, and network systems applications.

S3 is deploying SystemVerilog because it is the first and only non- proprietary language with broad industry support to enable an advanced verification methodology. The VMM for SystemVerilog gives S3 access to an open, proven methodology with a well-defined structure. The Synopsys VCS solution provides S3 with the best support for SystemVerilog through Native Testbench (NTB) technology, as well as for designs written in VHDL. These silicon-proven capabilities will reduce risk and enable predictable success for S3's designs across a wide range of applications.

"We support SystemVerilog and the VMM for SystemVerilog because non- proprietary verification solutions give us the flexibility we need to verify our broad range of system and silicon designs," said Dermot Barry, general manager, System IC Business Unit at S3. "The VCS verification solution and the Native Testbench technology for SystemVerilog, along with the proven verification concepts detailed in the VMM for SystemVerilog, are a powerful combination that gives us a high-performance, low-risk solution for our leading-edge silicon products."

SystemVerilog is a major extension of the established Verilog language that dramatically improves productivity in the development of large-gate- count, intellectual property-(IP) based, bus-intensive chips. SystemVerilog is targeted primarily at the chip implementation and verification flow, with powerful links to the system-level design flow.

"S3 adopted SystemVerilog and the VMM for SystemVerilog because they provide a stable, open-standard language and methodology to address S3's verification challenges for both VHDL and Verilog designs," said George Zafiropoulos, vice president of Marketing, Verification Group at Synopsys. "Because the VCS solution provides high performance through its Native Testbench technology and full support for the VMM for SystemVerilog, it has become the preferred solution for advanced verification using the standard language."

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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Editorial Contacts:

Isela Warner
Synopsys, Inc.
650-584-1644
igamboa@synopsys.com

Khyati Shah
Edelman Public Relations
650-429-2769
khyati.shah@edelman.com
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SOURCE: Synopsys, Inc.

CONTACT: Isela Warner of Synopsys, Inc., +1-650-584-1644, or igamboa@synopsys.com; or Khyati Shah of Edelman Public Relations, +1-650-429-2769, or khyati.shah@edelman.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/
