ADVISORY/Synopsys to Deliver Keynote, Lead SystemVerilog Tutorials at DVCon 2006

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that John Chilton, senior vice president and general manager of Synopsys' Solutions Group, will deliver the keynote at the Design and Verification Conference (DVCon) in San Jose, California on February 23, 2006. The conference's general chair is Karen Bartleson, director of interoperability, also of Synopsys. In addition, the company will deliver SystemVerilog tutorials and functional verification papers that address the requirements of achieving first-pass system-on-chip (SoC) silicon success.

WHAT: Highlights of Synopsys participation at DVCon. DVCon is the premier conference on the usage of Hardware Description Languages (HDLs), and Hardware Verification Languages (HVLs) for the design and verification of electronic systems and integrated circuits.

WHEN: February 22-24, 2006

WHERE: DoubleTree Hotel in San Jose, Calif.

DVCon Participation Highlights Include:

-- Keynote Address - Skyscrapers and Chip Design
Thursday, February 23, 2:00 PM - 3:00 PM
In his keynote, John Chilton will share insights on design productivity based on data gathered from real design projects. Chilton will address the influencers of design productivity -- many that you will recognize, and others that may surprise you.

-- DVCon Steering Committee
General Chair: Karen Bartleson, director of Interoperability, Solutions Group of Synopsys.

-- SystemVerilog Tutorials
Wednesday, February 22, 8:00 AM - 12:00 PM
Using the Verification Methodology Manual (VMM) for SystemVerilog
Presenters: Industry verification expert Janick Bergeron of Synopsys and Jonathan Bromley of Doulos.

Wednesday, February 22, 1:00 PM - 5:00 PM
SystemVerilog Assertions, From Concepts to Practice
Presenters: Verification experts Eduard Cerny of Synopsys and Faisal Haque, Jon Michelson and Khizar Khan of Verification Central LLC.

-- Technical Papers
Thursday, February 23, 9:15 AM - 10:45 AM
Transaction-Level Functional Coverage in SystemVerilog
Presenters: Janick Bergeron of Synopsys and Hans van der Schoot of XtremeEDA Corp.

Friday, February 24, 10:30 AM - 12:00 PM
Managing Capacity Limitations during Formal Verification of Assertions
Presenters: Jin Hou and Dan Benua of Synopsys.

-- Synopsys Booth
Wednesday, February 22 - Thursday, February 23, 4:00 PM - 7:00 PM
Synopsys will demonstrate its VCS® comprehensive RTL verification solution and VCS Verification Library of verification IP in booth #408.

-- Synopsys Cocktail Reception in the Exhibit Area
Wednesday, February 22, 5:00 PM - 7:00 PM
Presenter: George Zafiropoulos, vice president of Marketing, Verification Group of Synopsys.

For more information on DVCon, please visit:
http://www.synopsys.com/news/events/conference06/dvcon06.html

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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