Synopsys' coreAssembler Reduces Time and IP Integration Risk for Spirit-Compliant IP

Benefits Include Support for SPIRIT 1.0 Standard and Integration With Galaxy™ and Discovery™ Platforms

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Synopsys' coreAssembler intellectual property (IP) integration tool supports the SPIRIT 1.0 IP packaging standard. coreAssembler is the only tool that supports a path to implementation in silicon for SPIRIT-compliant IP in addition to system-level integration and verification. Tight integration with the Synopsys Galaxy Design Platform and Discovery Verification Platform helps to achieve superior quality-of-results and speed the time to verification. By providing production support for SPIRIT 1.0, coreAssembler now enables designers to more rapidly integrate the broad portfolio of DesignWare® IP, as well as third-party IP compliant with the SPIRIT standard.

Synopsys is a founding member of the SPIRIT consortium, an independent organization focused on defining standards for IP packaging and reuse. The SPIRIT 1.0 specification, released in December of 2004, defines a common, XML-based format to describe IP that is targeted for automated integration techniques and enables SoC integrators to use IP from multiple sources with SPIRIT-compliant tools.

coreAssembler is proven to reduce SoC design time by up to 67 percent by automating much of the work needed to integrate IP blocks into a SoC. It also reduces design risk by ensuring that the IP is correctly connected and configured. Using coreAssembler, designers can more rapidly and reliably integrate configurable IP subsystems, platforms and system-on-chip (SoC) designs. coreAssembler connects IP, facilitates verification and automates implementation with its built-in interfaces to the Galaxy and Discovery Platforms. By automatically generating a verification testbench using IP-specific generators, coreAssembler can reduce the time to verification from weeks to hours.

In addition to enhancing coreAssembler, Synopsys has also added SPIRIT 1.0 support to its coreBuilder IP packaging tool. coreBuilder enables designers to package IP and then automatically generate the SPIRIT 1.0 XML that describes the IP for use with IP integration tools like coreAssembler.

"Synopsys' support of SPIRIT with coreAssembler advances the SoC implementation flow for the industry," said John Goodenough, director of Design Technology at ARM. "Synopsys' support of SPIRIT enables engineers to smoothly migrate their designs to leading industry solutions at each stage of their design process."

"By adding SPIRIT support to the latest release of our coreAssembler tool we have enabled SoC designers to quickly assemble and implement SoC subsystems from IP building blocks that have been packaged following the SPIRIT standard," said Joachim Kunkel, vice president of engineering, DesignWare IP at Synopsys. "Furthermore, the latest release of coreBuilder helps IP developers package their IP such that it conforms to the evolving SPIRIT standard. This will significantly accelerate the availability of SPIRIT-compliant IP building blocks."

"It is gratifying to see the work done by Synopsys to provide a full implementation path to silicon for SPIRIT IP in their production products," said Ralph von Vignau, SPIRIT chairman. "Synopsys has strongly supported the creation of the SPIRIT standards and allowed SPIRIT member companies using Synopsys'

coreAssembler product to provide "proof of concept" and validation of the SPIRIT 1.0 specification."

Availability

The coreAssembler and coreBuilder products are currently available with SPIRIT 1.0 support.

About DesignWare IP

Synopsys' DesignWare IP enables designers to more cost effectively create and verify complex SoCs, ASICs and FPGAs. The broad IP portfolio includes industry leading connectivity IP cores and Verification IP (e.g., USB 1.1, 2.0, OTG and PHYs, PCI, PCI-X®, PCI Express™, PCI Express PHY, Ethernet, IEEE 1394, SATA, I2C), AMBA™ protocol on-chip bus (logic, peripherals, verification IP) complete memory solution (e.g., memory controllers, BIST and models), high-speed datapath components, microcontrollers (8051, 6811) and Star IP such as IBM PowerPC® 440, Infineon C166™S and TriCore®1, MIPS32™ 4KE™ and NEC V850E™ processors and Philips CoolFlux™ DSP core. When combined with our robust IP development methodology, extensive investment in quality and comprehensive worldwide technical support, DesignWare IP gives designers a faster, more predictable and lower-risk path to chip success. For more information on DesignWare IP visit: www.designware.com.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

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