Synopsys Provides Low-Power Reference Flow for IBM-Chartered 90-Nanometer Process Platform

Complete RTL to Production-Ready GDSII Flow Speeds 90-nm Designs

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced it is collaborating with IBM and Chartered Semiconductor Manufacturing to offer a low-power reference flow for the 90-nanometer (nm) common process platform. The Galaxy™ Design and Discovery™ Verification platforms are the foundation of the reference flow, extending the existing solution by addressing power reduction, signal integrity and design for manufacturing (DFM) issues.

Power reduction is one of the largest challenges facing 90-nm designers, and the reference flow is a proven methodology that takes advantage of the EDA tools and process technology to give designers a lower-risk path to low-power silicon. The Synopsys approach uses implementation tools, verification tools and IP to provide a complete solution for designing high performance, low-power 90-nm digital devices. ARM® Artisan® Metro™ low-power libraries are used for the flow development. Based on the production-proven design flow used by Synopsys Professional Services, designers can improve their time to results and reduce the cost of their products by encapsulating methodologies and subflows, command sequences and best practices in an easy-to-use approach.

Advanced Capabilities

The low-power Synopsys reference flow spans the complete design process. The JupiterXT™ design planning tool performs power network synthesis and analysis, storing its results in the Milkyway™ database. Utilizing the multiple threshold voltages and clock gating cells available in 90-nm low-power libraries, the Physical Compiler®, DFT Compiler™ and Power Compiler™ tools perform physical synthesis with timing-aware test insertion while simultaneously optimizing clock and data signal switching power, leakage power, performance and area. Full chip power analysis is supported by the PrimePower power analysis tool. The Astro™ detailed router completes the low-power timing closure process while also taking into account signal integrity, electro-migration and DFM guidelines. Final design sign-off is supported by the PrimeTime® SI, Star-RCXT™ and Hercules™ tools using a common set of technology files available from IBM and Chartered. Manufacturing test pattern generation and diagnosis is supported by the TetraMAX® ATPG product. Verification is addressed by the Discovery Platform, including the VCS® RTL verification solution for multi-language functional verification, the Formality® equivalence checking tool, and the HSPICE® circuit simulator. A broad range of compatible implementation and verification IP is also available through the DesignWare® Library.

"Low-power solutions are an increasingly important aspect for our customers and platform members," said Steve Longoria, vice president, Semiconductor Technology Platform for IBM. "The Synopsys low-power reference flow for our 90-nm common platform enhances customer choice and is further evidence of our intent to provide a comprehensive, open and broad-based offering to the marketplace."

"The 90-nm process platform we have developed with IBM is well suited to a wide range of applications. Synopsys provides key enabling design technologies that should help our customers quickly and confidently design their devices while realizing the full capabilities of the IBM-Chartered common process platform," said Kevin Meyer, vice president of worldwide marketing at Chartered. "In addition, Synopsys brings recognized expertise in timing closure, power optimization and DFM to the design effort with their low-power reference flow."

"We have been working with IBM and Chartered for many years to provide complete solutions for our customers. This reference flow combines expertise from all three companies, allowing designers worldwide to more easily take full advantage of our advanced low-power technologies," said Glenn Dukes, vice president, Synopsys Professional Services, Synopsys. "This reference flow enables designers to become productive more quickly by leveraging the infrastructure we are providing. As a result, they get their parts to market faster and at a lower cost using flows developed by Synopsys Professional Services. We are now extending these techniques to the IBM-Chartered family of 90 nanometer processes on the common platform to give designers access to the full capabilities of these process technologies."

Availability

The block-level reference flow is expected to be available by early third calendar quarter of 2005.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The Company delivers technology-leading semiconductor design and verification platforms to the global electronics market, enabling the development of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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