Synopsys, Inc. Announces Technical Seminar Series Featuring Mixed-Signal, Functional Verification, and Implementation Solutions

PRNewswire

Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced the commencement of its annual technical seminar series. From RTL to silicon, Synopsys provides solutions to the most difficult challenges that confront engineers who are pushing electronic design to the limit.

WHAT: The Synopsys 2004 Seminar Series is a forum for members of the electronic design community to get the most recent information on design automation products, methodologies and processes. Intended for designers, developers, verification engineers and managers, these free in-depth technical sessions discuss the latest technological advances and future trends of Synopsys' leading EDA tools and solutions for mixed-signal design, functional verification and implementation.

Synopsys 2004 Seminar Series includes:

Mixed-Signal
The AMS seminars offer customers the opportunity to learn about Synopsys' AMS design environment beginning with the Cosmos™ design cockpit and its integration with simulation solutions. The Discovery™ AMS solution demonstration, built around industry-leading golden simulators: VCS™, NanoSim™, and HSPICE®, will show attendees how to achieve the high verification throughput needed for AMS SoC designs. An efficient, high-quality post-layout simulation flow that combines the strengths of NanoSim and Star-RCXT™, Synopsys' parasitic extraction tool, is also covered. In addition, the Design Optimization section will explore exciting new technology that allows designers to quickly converge to an optimal circuit solution, offering significant productivity gains.

Functional Verification
As verification challenges continue to grow faster than chip complexity, new methodologies must be used to ensure first-pass silicon success. Synopsys' functional verification seminars will feature an advanced methodology developed by industry expert Janick Bergeron, moderator of Verification Guild and a Synopsys principal R&D engineer, that addresses the immense challenge of verifying today's complex designs. Attendees will learn how to architect a scalable, reusable verification environment that takes advantage of the latest advances in constrained-random and design-for-verification solutions to maximize productivity. Janick Bergeron will be a guest speaker at various worldwide locations.

Implementation
The challenges of chip design continue to increase; therefore the need for an implementation platform that is comprised of best-in-class tools is more critical to design success than ever before. The Implementation seminars are offered in two topic areas covering logical design and physical design. Attendees will receive useful design tips from the latest software releases that they can apply immediately for better management of their complex designs, improved productivity and best overall results.

For more information and to register, visit
http://www.synopsys.com/links/seminars_pr.html

WHEN: Beginning February, 2004. Dates and times vary worldwide.

WHERE: Worldwide locations include: Asia-Pacific, Canada, Europe, Japan and the USA.

WHO ATTENDS: EDA designers, developers, verification engineers and managers.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading IC design and verification platforms to the global electronics market, enabling the development of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

NOTE: Synopsys and HSPICE are registered trademarks and Cosmos, Discovery, NanoSim, Star-RCXT, and VCS are trademarks of Synopsys, Inc. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

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