Springer Publishes ARM-Synopsys Verification Methodology Manual for SystemVerilog

New ARM-Synopsys Book Provides Blueprint for System-on-Chip Verification Success Using SystemVerilog

PRNewswire-FirstCall
NEW YORK

Springer Science + Business Media, Inc., a major publisher of professional books and research journals in engineering, today announced the publication of the Verification Methodology Manual (VMM) for SystemVerilog, which was co-authored by ARM (LSE: ARM)(LSE: Nasdaq:)(LSE: ARMHY), and Synopsys, Inc. (NASDAQ: SNPS). The book, written by verification experts Janick Bergeron and Eduard Cerny of Synopsys, and Alan Hunter and Andrew Nightingale of ARM®, documents years of know-how and industry best practices for architecting advanced, efficient verification environments using industry-standard SystemVerilog assertions, testbenches and functional coverage. It also provides developers with specifications for a library of verification functions to speed development and enable interoperable verification components. The VMM for SystemVerilog, reviewed by verification engineers from over 30 semiconductor industry companies, helps enable chip development teams to achieve measurable functional coverage goals in less time with less effort, giving verification engineers and managers the confidence to tape out complex system-on-chip (SoC) and silicon intellectual property (IP) designs.

"System Verilog is a widely supported language in the silicon chip design industry, which is important to silicon IP companies such as ARM," said Tim Holden, director of EDA relations, ARM. "The Verification Methodology Manual for SystemVerilog addresses the industry's need for open methodologies to implement a coverage-driven verification environment based on an industry- standard language. We expect the manual will appeal to verification engineers everywhere, including those implementing ARM®technology-based designs, and provide the foundation for improved functional verification throughout the electronics industry."

Faster and More Predictable Verification with the VMM for SystemVerilog

The VMM for SystemVerilog addresses key aspects of functional verification, including the use of design-for-verification techniques with formal analysis, simulation and SystemVerilog assertions, constrained-random stimulus generation techniques, and coverage metrics to achieve rapid verification closure. The techniques are applicable to a wide variety of designs and can be implemented with SystemVerilog, an industry standard language. The manual also includes the complete specification for a standard set of libraries for assertions and commonly used verification functions. These assertions and verification functions include stimulus generation, simulation control and coverage analysis to speed implementation of an advanced verification environment using SystemVerilog.

"The Verification Methodology Manual for SystemVerilog is a blueprint for developing an effective and predictable verification strategy," said Seiichi Nishio, Sr. manager of Design Methodology at the Toshiba Corporation Semiconductor company in Japan. "It provides details and techniques on implementing advanced capabilities to build modern, interoperable coverage- driven verification environments based on SystemVerilog that enable faster and more effective verification."

"Just as the Reuse Methodology Manual (RMM) for System-on-a-Chip Designs established the open, industry standard for design reuse and reusable silicon IP, the Verification Methodology Manual for SystemVerilog defines an open, industry standard for advanced verification and interoperable VIP with SystemVerilog," said Farhad Hayat, vice president of Marketing, Verification Group, Synopsys, Inc. "The book enables designers to establish a more effective, efficient and predictable verification process for SoC and IP projects that is based upon the experience of leading verification experts from ARM, Synopsys and the electronics industry."

The authors will be signing books at special events at the Synopsys Users Group (SNUG) on Tuesday, September 27, 2005, in Newton, MA and at the ARM Developers' Conference in Santa Clara, CA on Thursday, October 6, 2005. Doulos, a global leader for training solutions for electronics development, will deliver a free, introductory technical tutorial on the VMM for SystemVerilog at both events. Seating for these tutorials is limited, so early registration is advised. More information on these events is available at www.vmm-sv.com.

Pricing and Availability

The Verification Methodology Manual for SystemVerilog is available now from Springer for $129.00 U.S. For more information or to order the book online, please visit www.springeronline.com/0-387-25538-9 or www.vmm-sv.com.

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