Synopsys Partners With TSMC to Offer Comprehensive DFM Solution for Yield Enhancement

Complete Tool Suite From TCAD to Design to Mask Synthesis Enables Yield Enhancement Concurrently With Area, Timing and Power Optimization

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Taiwan Semiconductor Manufacturing Company Ltd. (TSMC) (NYSE: TSM; TAIEX: 2330) included Synopsys' integrated Design for Manufacturing (DFM) tools suite in its DFM tool qualification program for enhancing yield during design.

New DFM-compliance capabilities include Lithography Compliance Checking (LCC), Critical Area Analysis (CAA), and CMP (Chemical Mechanical Polishing) modeling, simulation and extraction -- all integrated with design implementation. This adds to Synopsys' existing production-proven capabilities for improving manufacturability of physical design using the IC Compiler physical design solution, physical verification using the Hercules™ physical verification product, mask synthesis using the Proteus optical proximity correction (OPC) product, and process development and optimization with TCAD tools. The complete flow is critical in addressing the increasingly complex interplay between design yield and the traditional metrics of area, timing and power.

"The Synopsys DFM flow is a result of a technical relationship between the two companies to deliver on an integrated approach for tackling systematic and random yield effects," said Edward Wan, senior director of Design Service Marketing at TSMC. "This decreases time to market and increases productivity and yield."

Lithography errors are a major source of systematic yield problems. TSMC and Synopsys worked to ensure that the accuracy of Synopsys' DFM-LCC technology matches that of TSMC's production flow by flagging potential lithographical errors and process variation effects for the designer earlier in the design process. With its advanced architecture, the DFM-LCC technology delivers fast runtimes and uses less memory for layouts ranging from library cells up to the biggest designs. The technology also delivers superior predictability with production-quality silicon correlation from the Proteus OPC tool. To boost designer productivity, DFM-LCC links to the leading routing tool, IC Compiler, for automated correction of lithographical errors.

Particle-induced defects are a leading cause of random yield loss. To enable the optimization earlier in the design flow, Synopsys and TSMC worked closely to qualify the Critical Area Analysis (CAA) engine in IC Compiler to provide excellent correlation with the TSMC internal reference data. IC Compiler takes a particle distribution as input and displays critical areas with higher probability of yield loss in the layout. The tool then applies a complete wire-spreading and wire-widening methodology to reduce the average critical area and increase yield while preserving timing.

Uneven metal fill is a major source of systematic failures in advanced chip design. The two companies validated the accuracy of DFM-CMP modeling and simulation results for full chip thickness variation analysis. The IC Compiler tool uses the analysis results from DFM-CMP to provide model-based dummy metal filling in order to fix potential issues from metal variations caused by the CMP process.

"TSMC has a well-known reputation for providing production proven, leading-edge manufacturing flows for its many customers," said Anantha Sethuraman, vice president of marketing for Design for Manufacturing, Silicon Engineering Group, Synopsys. "The selection of our tools for the TSMC DFM flow speaks to their quality, reliability, and accuracy. We have worked closely with TSMC to qualify our tools for yield analysis and enhancement during and after design implementation."

About Synopsys DFM

With its DFM tools, Synopsys is expanding on what is already the industry's most comprehensive design for manufacturing (DFM) solution that spans from RTL to silicon. Synopsys' DFM product family addresses critical manufacturability and yield issues with the following products: IC Compiler physical design solution, DFM-LCC, DFM-CMP technologies, Hercules™ physical verification tool, Proteus OPC, CATS® mask data preparation product, SiVL® lithography verification tool, patented PSM technology, and physics-based TCAD suite of simulation products. Synopsys' Manufacturing Yield Management (MYM) solutions extend directly into the fab, providing customers real time access to yield data and the analysis capability needed to reduce random, systematic and parametric defects.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com .

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits of Synopsys' DFM compliance capabilities. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties in final deployment of these technologies on TSMC's processes and uncertainties attendant to any new manufacturing process technology, as well as certain statements contained in the section of Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended January 31, 2006 entitled "Management's Discussion and Analysis of Financial Condition and Results of Operations -- Factors That May Affect Future Results."

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