16 Synopsys Technologists Recognized for Leadership in Creation of SystemVerilog Standard

IEEE Working Group Chairman Awards and Certificates of Recognition Presented to Synopsys Engineers

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that the Institute of Electrical and Electronics Engineers (IEEE) has presented its Working Group Chairman's Award to two Synopsys technologists and certificates of recognition to 14 other Synopsys engineers for their key contributions in the development of the SystemVerilog standard (IEEE Std. 1800-2005). Dr. Karen Pieper and Dr. Brad Pierce received the Chairman's Award. Certificates of recognition were presented to: Ms. Tapati Basu, Dr. Ed Cerny, Dr. Surrendra Dudani, Dr. Mark Hartoog, Mr. Greg Jaxon, Mr. Ghassan Khoory, Mr. Oz Levia, Dr. Andrzej Litwiniuk, Mr. Mehdi Mohtashemi, Mr. Sachchidananda Patel, Dr. Loganath Ramachandran, Dr. Arturo Salz and Mr. Arif Samad.

Synopsys donated key technologies to the development of the SystemVerilog standard, including testbench, assertions and C language integration. Synopsys also provided significant technical resources to the various technical committees starting with its early work with standards body Accellera and continuing through to the recent IEEE standardization. Synopsys is a leader in the electronic design automation (EDA) industry in providing tool support for SystemVerilog in its Galaxy™ Design and Discovery™ Verification platform tools, including Design Compiler® RTL synthesis product, VCS® RTL verification solution, Formality® equivalence checking tool, LEDA® RTL rule checking tool, Magellan™ hybrid formal analysis product and Pioneer-NTB testbench solutions.

"On behalf of the IEEE Std. 1800-2005 SystemVerilog Working Group, I would like to thank Synopsys and its technologists for their dedication and help in making SystemVerilog one of the most successful standards in EDA history," said Johny Srouji, chair of the IEEE 1800 SystemVerilog Working Group. "Synopsys' support and the expertise of its engineers made the standard come together quickly, so that design engineers can use the SystemVerilog language for their next-generation designs."

"Synopsys is honored to be recognized for its technologists' contributions to the IEEE SystemVerilog standard," said Raul Campasano, senior vice president and chief technology officer at Synopsys. "Our engineers worked hard on the development of SystemVerilog and made sure that the standard will fit seamlessly into designers' existing flows. Synopsys will continue to participate in enhancement efforts for future versions of SystemVerilog."

Availability

The SystemVerilog standard is available now for product development and engineering use and may be purchased from the IEEE at: https://www.techstreet.com/publishers/ieee

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process

and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com .

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