STMicroelectronics Cuts Verification Time in Half With Synopsys' VCS RTL Verification Solution

Comprehensive Built-in Coverage Metrics in Synopsys' VCS® Solution Increase Verification Quality for STMicroelectronics' 90 Nanometer HDTV Processor Chip

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced its VCS® comprehensive RTL verification solution, a key component of the Discovery™ Verification Platform, enabled STMicroelectronics to achieve its verification quality goals in half the time for its next-generation 90 nanometer STD2000 family of HDTV processor chips. STMicroelectronics used VCS' high-performance, built-in coverage technology to help ensure verification completeness and to increase confidence in the quality of the 10 million-gate design targeted at television applications.

"We chose the VCS solution because it delivers the highest performance for the implementation of our coverage-driven verification environment," said Sebastien Francois, verification manager at STMicroelectronics. "Our comprehensive regression suite tracks various coverage metrics to determine verification progress. With built-in, comprehensive coverage metrics, the VCS solution provides the performance and the breadth of coverage technologies required to achieve our verification goals in the given time."

Faster Time to Results with VCS Coverage-Driven Verification

The VCS solution delivers comprehensive coverage metrics, including functional, assertion, finite state machine, condition, path and toggle. These coverage metrics are natively compiled in the VCS solution to deliver faster performance and to increase productivity by eliminating the need to instrument the design. Additionally, the VCS solution provides the following critical coverage capabilities:

-- Auto-grading of coverage achieved from multiple tests, allowing designers to eliminate inefficient or redundant tests, saving wasted regression cycles
-- Aggregation of reports from multiple regression runs to easily review total achieved coverage value
-- Flexibility to turn on or off coverage tracking, saving valuable throughput time

"We have expanded VCS from an HDL simulator into a comprehensive mixed-language RTL verification solution to enable customers designing complex chips, such as STMicroelectronics STD2000 family, to complete RTL verification tasks in less time," said Farhad Hayat, vice president of Marketing, Verification Group, Synopsys, Inc. "We continue to see rapid customer adoption of the built-in VCS bug-finding technologies, such as Native Testbench, comprehensive coverage and complete assertions."

About VCS

The Synopsys VCS comprehensive RTL verification solution, a key component of the Discovery Verification Platform, provides high-performance, powerful bug-finding technologies targeted at the functional verification of complex SoCs. The VCS solution supports industry-standard design and verification languages including Verilog, VHDL, SystemVerilog, SystemC™ and OpenVera®. Powerful built-in bug-finding technologies include Native Testbench, comprehensive coverage analysis and complete assertion support. VCS' single-compiler architecture enables design, testbench and assertions to be compiled, optimized and executed together in a single tool.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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