Synopsys Extends VCS With Full-Featured Built-In Testbench Technology

Expanded Testbench and Assertion Capabilities Find Complex Design Bugs and Deliver Significant Performance Improvement

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Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced the latest release of the VCS® RTL verification solution. VCS, a key component of the Discovery™ Verification Platform, extends its built-in testbench capabilities to include a rich set of advanced technologies for RTL verification. These advancements include support for the same next-generation constraint-solver engines used in the Vera® testbench automation tool, support for object-oriented testbench architecture, and advanced data types. With the addition of these new capabilities, engineers can use VCS to create and run powerful constrained-random testbenches using a single unified tool for maximum productivity and improved overall verification run time by up to five times, including simulation of design, testbenches and assertions, compared with standalone testbench tools working with VCS.

"We are continuously improving our verification methodologies," said Shrenik Mehta, director of Frontend Technologies, Scalable Systems Group at Sun Microsystems. "By using the testbench and assertion capabilities built into VCS, our engineers are able to write powerful testbenches that run faster compared to other standalone solutions from Synopsys, allowing us to run more verification cycles in the given time. This is extremely useful in reducing the development cycle as we design our next-generation Chip Multithreaded (CMT) processors for Throughput Computing."

Finding Design Bugs with Powerful Constraint-Solver Engines

VCS now has built-in support for the same proven, next-generation constraint-solver engines used in the Vera testbench automation product. The multiple solver engines simultaneously analyze all user-specified constraints to rapidly generate high-quality random stimulus to simulate the design for corner-case behavior. These engines will find a solution to user constraints, if one exists, minimizing constraint conflicts and maximizing verification productivity.

In addition to many testbench constructs already supported, other new built-in testbench technologies, natively supported in VCS, include:

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-- Support for object-oriented programming
-- Advanced data types, such as:
   -- Dynamic arrays
   -- Associative arrays
-- Random stream generation capability
-- Virtual ports
-- DirectC interface
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With the addition of object-oriented programming support in VCS engineers can create reusable and easily extendable testbench infrastructure. The addition of advanced data types improves verification productivity by allowing engineers to write compact yet powerful testbenches. The built-in stream generator in VCS can now be used to create random combinations of transactions or microprocessor instructions. This capability allows engineers to verify the design under numerous operating scenarios that are difficult to create manually, thus increasing the quality of the design.

"To deliver our highly integrated VLSI solutions used in global communications equipment, we verify our designs in many different configurations using constrained random testbench techniques," said Chris Kniker, principal member of technical staff at TranSwitch, a provider of high-speed VLSI semiconductor solutions. "By using the full-featured testbench capabilities in VCS, such as object-oriented programming and constraint-solver engines, we are able to deploy a comprehensive testbench environment to thoroughly verify our designs. Additionally, the built-in technologies in VCS have allowed us to run our regressions in half the time as compared to previous standalone approaches."

VCS natively compiles OpenVera™ testbench code into the simulation engine delivering up to five times speed up of the overall verification environment. The performance improvements are realized by applying VCS' advanced optimization algorithms to the combination of testbench and RTL code, as well as eliminating the communication overhead of separate testbench and HDL simulation tools.

"Our customers continue to require additional performance and capacity to meet the verification demands of their complex SoC designs," said Farhad Hayat, vice president of marketing at Synopsys. "By natively compiling the advanced Vera testbench technology into VCS, we continue to deliver higher performance and simulation capacity to enable our customers to meet their aggressive verification goals while finding more complex bugs in their designs."

Availability

All above enhancements are available immediately with the 7.1 release of VCS. For more information on VCS, please visit https://www.synopsys.com/verification/simulation/vcs.html .

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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