Synopsys' SiVL® Silicon-Versus-Layout Verification Tool Enhancements Enable Faster Time-to-Yield

SiVL Helps Prevent Months of Product Delay Through Accurate, Comprehensive Lithography Verification

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Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced substantial enhancements to SiVL, a silicon-versus-layout (SVL) verification tool and key component of Synopsys' design-for-manufacturing (DFM) solution. SiVL compares a target design to its simulated silicon image in order to verify that the design is manufacturable. Its proven silicon-correlated models, new 'check-figure' capability and enhanced checking functionality ensure that key lithography induced errors are identified, all of which are essential for resolution enhancement technology (RET) closure. RET closure is achieved when a design's layout matches its actual silicon image. Accurate lithography simulation reduces the risk of re-spins, which can save hundreds of thousands of dollars in scrapped materials and months in production delays.

"As part of UMC's commitment to design for manufacturability (DFM), we continue to lead in the implementation of the most advanced lithography technologies," said Kuan Liao, director of the CRD Advanced Module Division at UMC. "This has helped us to minimize the potential for mask error at very deep sub-micron generations. The SiVL verification tool is a welcome addition to our capabilities as we use it to support our 90 and 65 nanometer process technologies. The excellent model accuracy coupled with the 'check-figure' capability helps us maintain accurate error coverage to avoid costly prototype delays caused by lithography errors."

Expanded capability enables RET Closure

Compared to 130nm designs, 65nm designs have up to 30 times more complex mask synthesis due to increased layout, model, and RET recipe complexity. This increased complexity results in a proportional increase of the risk of lithography errors in mask and wafer fabrication. Finding these lithography errors in order to achieve RET closure requires accurate, full-chip simulation and high error coverage.

To obtain accurate full-chip simulation, SiVL utilizes the production-proven, highly accurate, modeling technology from Synopsys' Proteus® optical proximity correction (OPC) product. SiVL's unique 'check-figure' capability finds the critical features most likely to have errors before applying a combination of simulation-based lithography rule checks (LRC) to find real-world lithography errors. It also utilizes and pattern based checks, such as mask rule checks (MRC), to improve mask manufacturability. In order to achieve high error coverage, the checks are applied based on design style, feature-type and RET characteristics.

Accurate and thorough simulation based checking can be highly compute-intensive. In order to meet the turnaround-time challenge, SiVL uses an intelligent, automated methodology to apply simulation only to the most error-prone areas, significantly reducing the simulation burden. SiVL then distributes simulations using Synopsys' unique distributed processing capability that has been proven scalable in Synopsys' Proteus OPC tool when used on a compute platform containing over 1,000 processors.

"The rapidly expanding use of RET in the 90 and 65 nanometer nodes dramatically increases the chances of killer lithography-related defects going undetected -- which can easily result in weeks or months of product delay," stated Sandeep Khanna, vice president of marketing for Synopsys' Design for Manufacturing Group. "With the new version of SiVL, Synopsys is delivering a verification solution to find these defects to obtain RET closure and prevent such costly time-to-market delays."

About Synopsys DFM

Synopsys offers the industry's most comprehensive RTL-to-Mask Design-For-Manufacturing (DFM) solution. Its DFM product family addresses critical yield and manufacturability issues with its software products: Proteus mask synthesis, CATS™ mask data preparation, SiVL lithography verification, iVirtual Stepper™ mask defect dispositioning and Taurus™ TCAD. Synopsys leverages this expertise in its industry-leading Galaxy™ Design Platform implementation solution in order to help ensure that designs at 90nm and smaller geometries will meet key manufacturing requirements. Synopsys' DFM product family is the solution-of-choice at leading semiconductor manufacturers worldwide. More than eighty percent of all sub-180nm microprocessors, more than fifty percent of all DRAMs, more than eighty percent of all FPGAs, more than ninety percent of all graphics processors, and more than seventy-five percent of all cell phone baseband chips produced use Proteus, and more than seventy percent of all photomasks produced use CATS.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading IC design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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