Synopsys Delivers New FPGA Synthesis Solution to Solve the Toughest Prototyping Challenges

Design Compiler® FPGA Delivers Industry Standard ASIC-Strength Solution, Best Circuit Timing and Fastest Path to ASIC Prototype

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Synopsys, Inc. (NASDAQ: SNPS), the world leader in semiconductor design software, today announced Design Compiler® FPGA (DC FPGA), a new FPGA synthesis product targeted for designers who prototype ASICs using high-end FPGAs. Built upon Synopsys' Design Compiler technology and incorporating new Adaptive Optimization™ technology, DC FPGA provides designers with an industry standard ASIC-strength solution, the best circuit timing results, and the fastest path to a prototype, through a common ASIC and FPGA flow. To date, over 40 customers have purchased DC FPGA and 20 prototype designs have been successfully completed.

Today's ASIC designers are faced with a multitude of prototyping challenges. Most ASIC prototypes require the largest, most advanced FPGAs available. These FPGAs are extremely complex and need an ASIC-like methodology. Many of these ASIC prototypes are required to run at full speed, particularly for wireless designs, therefore timing quality-of-results (QoR) is critical. In addition, using incompatible synthesis solutions involves a time-consuming and error-prone manual effort to move designs between the ASIC and the prototype. Usually, RTL code, synthesis constraints, scripts and the ASIC IP must be changed, making this step as difficult as designing another chip.

In contrast, DC FPGA's compatibility with Design Compiler enables the integration of the ASIC and FPGA design environments. DC FPGA accepts the same RTL code, constraints, scripts, and IP libraries as Design Compiler, and provides the same interface to Formality® formal verification. This enables a seamless migration between ASIC and FPGA flows, eliminates manual changes and provides the fastest path to ASIC prototype. Designers prototyping using DC FPGA only need to design once, and benefit from the power of ASIC tools, like Formality, Leda®, PrimeTime® and the extensive DesignWare® libraries for their prototype.

"As a customer-centric designer and manufacturer of microprocessors, Flash memory devices and system-on-chip solutions for the computer and communications industry, AMD is pushing the speed limits of today's FPGA device technology," said Dirk Haentzschel, senior design engineer at AMD Dresden Design Center. "Using DC FPGA from Synopsys, we were able to meet the 40MHz wireless LAN 802.11g ASIC prototyping chip performance target -- a significant speed increase over what we were able to achieve with other FPGA synthesis tools. DC FPGA's compatibility with Design Compiler and the flexibility to run on a Linux-based platform significantly accelerates our design flow process by giving us access to a common design environment for both ASIC and FPGA design."

DC FPGA's Adaptive Optimization technology contains new, advanced optimizations that automatically activate the best core synthesis algorithms based on multiple parameters, including design size, circuit topology and timing constraints, then dynamically control and reorder how the algorithms are applied. The resulting circuits produced by DC FPGA operate, on average, 15 percent faster than those produced by traditional FPGA synthesis products.

"ASIC designers are increasingly adopting FPGAs for prototyping as part of their verification flow," said Tim Southgate, vice president of Software and Tools Marketing, Altera Corp. "With the introduction of Altera's high density Stratix II family, over 50 percent of ASIC design starts can now be prototyped on a single FPGA. While historically this required two separate design flows, the availability of DC FPGA now allows ASIC designers to use a single design environment."

"Synopsys' new Design Compiler FPGA combined with industry-leading FPGA technologies from Xilinx can deliver a significant cost savings and time-to-market advantage to our customers," said Rich Sevcik, executive vice president of the FPGA Products Group for Xilinx. "With DC FPGA's excellent timing performance and unified FPGA and ASIC design flow, Synopsys users can now realize the full potential of the Xilinx high-performance Virtex-II Pro and Spartan-3 devices."

"Over forty percent of our customers are prototyping their ASICs in FPGAs and they are faced with the challenge of meeting timing while designing with FPGAs that are as complex as ASICs," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "DC FPGA's innovative new optimization technology, combined with a design flow that is compatible with Design Compiler's ASIC flow, enables designers to focus on their ASIC designs and then easily and automatically target them to high performance prototypes."

Pricing and Availability

DC FPGA is currently available. A standalone license of DC FPGA starts at $36,750 for a one-year technology subscription license (TSL). Existing users of Design Compiler may purchase an add-on DC FPGA license for $19,600 for a one-year TSL.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading IC design and verification platforms to the global electronics market, enabling the development of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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