Key Synopsys Low Power and DFM Technologies Support TSMC Reference Flow 6.0

Synopsys' Galaxy Design Platform Provides Advanced Power Closure and Enhanced Yield Capabilities for Reference Flow 6.0

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, and Taiwan Semiconductor Manufacturing Company (NYSE: TSM) today announced the integration of Synopsys' Galaxy™ Design Platform, a complete RTL to GDSII solution into TSMC's Reference Flow 6.0(SM). Reference Flow 6.0 incorporates key Synopsys technologies that address design planning, low power management, dynamic voltage drop analysis, testability and design for yield and manufacturing (DFY/DFM) improvements at the 90-nm and 65-nm processes.

Galaxy's inclusion in Reference Flow 6.0 results from a long-standing collaboration between TSMC and Synopsys. It is based on a results-oriented approach to integrating semiconductor design and manufacturing that reduces risk and shortens time-to-results. This optimized approach aligns design tools and methodologies, mask creation, fabrication and test including IO package and advanced flip chip capabilities to handle high pin count designs to achieve common goals for final silicon.

Reference Flow 6.0 targets 90-nm and 65-nm designs, and addresses issues such as power closure and well proximity effects by linking together TSMC's advanced processes, libraries, and Synopsys' design platform to deliver the full benefits of TSMC's advanced technology features. Reference Flow 6.0 supports advanced low-power design methodologies such as multi-voltage, leakage power optimization, deep sleep (shutdown) mode and static/dynamic voltage-drop analysis. In addition, Synopsys' PrimeRail solution provides power network sign-off in the Reference Flow.

At 90 nm and below, yield is a key concern. Synopsys and TSMC have worked together to ensure manufacturing issues are considered at the beginning of the design phase and throughout the design cycle to improve yield. Synopsys' Astro™ tool provides the physical design capabilities in the Reference Flow and supports TSMC's 90-nm and 65-nm recommended design guidelines. To ensure testability for TSMC's complex deep submicron processes, Reference Flow 6.0 includes Synopsys' DFT MAX comprehensive design for test (DFT) synthesis solution.

"Over the years, Synopsys and TSMC have worked together to keep up with the evolving challenges of deep submicron design," said Ed Wan, senior director of design service marketing at TSMC. "With each generation of silicon complexity, new challenges arise. At 90- and 65-nanometer processes, manufacturability and yield take their place alongside timing and signal integrity as vital design concerns. Our Reference Flow 6.0 brings together the complete solutions of the Galaxy Design Platform and TSMC's latest process technology."

"We've worked closely with TSMC to ensure that our Galaxy Design Platform, with advanced DFM and low-power optimization technologies, offers the solutions that designers need to address complex, deep-submicron challenges," said John Chilton, senior vice president and general manager of Synopsys' Solutions Group. "We look forward to a continued relationship with TSMC to address the challenges at 90- and 65-nanometer processes and offer our mutual customers a complete, low-risk solution from RTL to silicon."

About TSMC Reference Flow 6.0 Support

Reference Flow 6.0 incorporates a complete Synopsys-based RTL-to-GDSII solution utilizing the Galaxy Design Platform for RTL synthesis, physical implementation and sign-off, and the Discovery Verification Platform with VCS® and HSPICE® for RTL verification and circuit simulation. As an integral part of the reference flow, extensive Galaxy support includes Design Compiler® logic synthesis solution, Power Compiler™ power management solution, DFT MAX 1-pass test synthesis solution, Jupiter-XT™ physical planning solution, Physical Compiler® and Astro physical implementation solutions, PrimeTime® and PrimeTime SI static timing and signal integrity sign-off solutions, PrimeRail power network sign-off solution, PrimePower full-chip power analysis solution, Star-RCXT™ parasitic extraction solution, Hercules™ PVS physical verification solution, and TetraMAX® automatic test generation (ATPG) solution. In addition, Synopsys Professional Services provides expertise in chip implementation and flow deployment services with Reference Flow 6.0.

About TSMC

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process

technology and the foundry industry's largest portfolio of process-proven library, IP, design tools and reference flows. The company operates two advanced twelve-inch wafer fabs, five eight-inch fabs and one six-inch wafer fab. TSMC also has substantial capacity commitments at its wholly-owned subsidiary, WaferTech and TSMC (Shanghai), and its joint venture fab, SSMC. In early 2001, TSMC became the first IC manufacturer to announce a 90-nm technology alignment program with its customers. TSMC's corporate headquarters are in Hsinchu, Taiwan. For more information about TSMC please see http://www.tsmc.com/ .

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http:/www.synopsys.com .

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