Synopsys' DFT MAX Cuts Test Time and Cost on CSR Bluetooth Designs

DFT MAX Adaptive Scan Technology Enables Predictability Through First-Silicon Success

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that CSR plc, a global provider of the hardware/software single-chip wireless solutions BlueCore™ for Bluetooth® applications and UniFi™ for 802.11/Wi-Fi/Wireless LAN, has successfully used Synopsys' DFT MAX to reduce digital tester costs. CSR needed a design-for-test solution that would meet its high quality goals, yet would be easy to implement and have minimal silicon area overhead. DFT MAX was deployed as part of the Synopsys Galaxy™ Design Platform and achieved 90 percent digital test time/test data reduction for several BlueCore designs. When the devices were fabricated, the test patterns were applied successfully to validate the silicon.

"We needed very high quality levels for our high-volume manufactured designs to minimize the number of field escapes," said James Collier, chief technical officer and co-founder of CSR. "At the same time, we wanted to avoid a corresponding increase in tester costs, if possible. Using DFT MAX to reduce digital test data volume by 90 percent, we were able to add DSM testing to our test suite to further increase quality without the need for expensive tester hardware upgrades. Moreover, reduction in test execution time achieved by DFT MAX actually decreased our overall tester costs."

CSR designers were also pleased to discover how easy it is to implement DFT MAX for scan compression. "Our team was optimistic about the cost benefits of using DFT MAX but anticipated it would take awhile to learn how to adopt it for production use," said Alan Duffy, CSR design engineer. "However, we got it working the first day just by adding a couple of lines to our synthesis scripts. It is unlikely we will undertake any more designs without using DFT MAX for scan compression."

Working seamlessly as part of the Galaxy Design Platform, DFT MAX predictably reduces test costs by up to 50x compared with traditional scan techniques. The key advantage of DFT MAX is that it is easy to implement and is far less intrusive on design flows and design performance than alternative solutions. The Galaxy platform delivers design engineers a single environment for synthesis, physical implementation, and sign-off. Concurrent optimization for timing, signal integrity, area, power, and test within the Galaxy environment helps eliminate costly and time-consuming design iterations between front-end and back-end flows.

"Designers are under immense competitive pressure to deliver high-quality parts at lower cost than ever before," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Simultaneously, designers must realize their quality and cost goals in shorter timeframes. To obtain predictable results quickly, the Galaxy Design Platform considers all the critical timing, signal integrity, area, and power effects of adding test logic to a design. DFT MAX helped CSR achieve its test goals in record time."

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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Editorial Contacts:
Janet Berkman
Synopsys, Inc.
650-584-5707
jberkman@synopsys.com

Angela Costa
Edelman
650-429-2765

angela.costa@edelman.com

SOURCE: Synopsys, Inc.

CONTACT: Janet Berkman of Synopsys, Inc., +1-650-584-5707, or jberkman@synopsys.com; or Angela Costa of Edelman, +1-650-429-2765, or angela.costa@edelman.com, for Synopsys

Web site: http://www.synopsys.com/