Industry Momentum Builds for the ARM-Synopsys VMM for SystemVerilog

Users Embrace the VMM Methodology for SystemVerilog and Synopsys' VCS® Native Testbench

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that industry adoption and support of the Verification Methodology Manual (VMM) for SystemVerilog, co-authored by ARM and Synopsys, has steadily increased since the book's release in September 2005. The resulting momentum has established the VMM as the industry's most mature and proven methodology for SystemVerilog, making the VCS® Native Testbench (NTB) solution the leading platform for deploying SystemVerilog-based environments. Recent highlights of this momentum include adoption of the VMM methodology using VCS NTB, licensing of the free VMM Standard Library source code and an expanding ecosystem of training and companion publications.

"The VMM methodology provides a powerful, robust and open approach to creating SystemVerilog verification environments more quickly and easily," said Alan Sherman, principal member of technical staff at Vitesse. "The easy access to Synopsys' implementation of the VMM Standard Library source code has given us additional insight into the methodology and will help ensure project portability across multiple EDA tools."

Synopsys provides its implementation of the VMM Standard Library, the building block library defined in VMM for SystemVerilog, as a standard feature of its VCS solution to help speed deployment of VMM-based environments. To reinforce the open nature of the VMM methodology, Synopsys also makes licenses available, at no additional cost, to customers and SystemVerilog Catalyst program members for the source code of Synopsys' implementation of the VMM Standard Library. Many end-user companies and EDA vendors have licensed the source code.

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The VMM for SystemVerilog defines industry best practices for coverage-driven, transaction-level verification incorporating constrained-random stimulus generation, assertions and functional coverage. With full support for the VMM methodology, VCS NTB has been adopted by leading-edge system-on-chip (SoC) developers to achieve higher verification performance and productivity. Several recent Synopsys press releases have described this adoption and success, while 15 papers and presentations at recent Synopsys Users Group (SNUG) events have discussed experiences and success with the VMM methodology and the VCS NTB solution.

"VCS gives us a powerful, comprehensive solution for SystemVerilog-based design and verification," said Steve Blightman, founder and manager of ASIC development at Alacritech. "We are taking full advantage of the VCS solution's support for the VMM methodology, the VCS Verification Library, powerful constraint solvers and integrated testbench debug environment to complete our verification tasks more productively. The VMM methodology in particular helps us create a more consistent verification environment that will lower the learning curve for new members joining our team in the future."

VMM Methodology Ecosystem Expands

The advanced techniques detailed in the VMM for SystemVerilog deliver tremendous value in terms of

verification productivity and predictability, but some training is helpful at making adoption as quick and easy as possible. Four related publications provide more background on the concepts and language behind the methodology and offer advice on adoption and deployment. These publications include Writing Testbenches Using SystemVerilog by Synopsys author Janick Bergeron; A Pragmatic Approach to VMM Adoption from verification authors Ben Cohen, Srinivasan Venkataramanan and Ajeetha Kumari; SystemVerilog for Verification by Synopsys author Chris Spear; and the VMM Companion Guide from Doulos Ltd. and Synopsys.

"Based on first-year sales volume, the VMM for SystemVerilog is one of the fastest-selling EDA-related books we have ever published," said Carl Harris, senior editor, Springer. "This success has spawned a series of complementary books that show that the VMM methodology is becoming a broad industry phenomenon."

In addition to these publications, numerous Synopsys and third-party educational opportunities are now available to help verification teams get up to speed quickly. Synopsys' Customer Education Services offers a new two-day VMM methodology course as part of its standard training menu; Synopsys' Worldwide University Program makes SystemVerilog and VMM methodology training material available for use in academic settings.

Professional training providers such as methodology specialist Doulos are also lining up to support the VMM methodology. Available now, within its "Modular SystemVerilog" training program, Doulos includes the "VMM Companion Class" to address the needs of project teams gearing up with VMM. In addition, Sutherland-HDL offers a two-day workshop, "Practical Application of the Verification Methodology Manual Using SystemVerilog." Within academia, the University of California Extension, Santa Cruz is offering a new 10-week course "SystemVerilog VMM Verification Methodology" starting on September 21.

"The VMM methodology defined by ARM and Synopsys lead verification engineers is being followed with great success by many in the electronic design industry," said Keith Clark, vice president, Technical Marketing, ARM. "Worldwide demand for the methodology is strong, prompting translation of the VMM book into Japanese and other languages in order to further the availability in these design communities."

"The growing VMM methodology user community and vendor ecosystem is strong acknowledgement of broad market adoption of open methodologies based on the widely supported SystemVerilog standard," said Manoj Gandhi, senior vice president and general manager, Verification Group at Synopsys, Inc. "The VMM methodology incorporates the contribution of verification experts from more than 30 semiconductor industry companies around the world. It builds upon the high-performance VCS NTB technology, enabling a new wave of verification productivity and predictability."

For more information on Synopsys SystemVerilog solutions please visit www.synopsys.com/systemverilog. To register for the SystemVerilog User Forum Luncheon taking place on Tuesday, July 25, demos and a VMM book-signing event with authors Alan Hunter and Andrew Nightingale from ARM and Janick Bergeron and Eduard Cerny from Synopsys at the Design Automation Conference at the Moscone Center in San Francisco, CA, please visit: www.synopsys.com/dac.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe,

Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

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