Virage Logic Adopts Synopsys' HSPICE Simulator as Golden Simulator for 65-nm Library Sign-off

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Virage Logic Corp. (NASDAQ: VIRL), a pioneer in Silicon Aware IP™ and leading provider of semiconductor IP platforms, has adopted Synopsys' HSPICE simulator® circuit simulator as its sign-off simulator for library characterization.

"Virage Logic has a longstanding reputation of providing high quality, silicon proven IP that helps customers accelerate their silicon success. The selection of HSPICE simulator as our golden sign-off simulator for all of our 90-nanometer (nm) and below ASAP Logic libraries helps ensure the accuracy, performance and wide foundry acceptance that our customers have come to expect," said Jim Ensell, senior vice president of marketing and business development for Virage Logic.

HSPICE simulator helps Virage Logic achieve accurate timing characterization for their Area, Speed and Power (ASAP) Logic™ Standard Cell Library products implemented in 90- and 65nm. Virage Logic's ASAP Logic libraries are widely used by customers developing new designs with Synopsys' Galaxy™ Design Platform. Customers using Synopsys tools benefit from predictable quality of results due to high-accuracy libraries.

"Synopsys continues to invest in HSPICE simulator with performance enhancements that extend its position on the leading edge of silicon-accurate simulation technology," said Ravi Tembhekar, vice president of AMS marketing and application engineering at Synopsys. "Our joint customers benefit by access to higher quality libraries as a result of Virage Logic's use of HSPICE simulator to create their next-generation products."

About The Virage Logic ASAP Logic Product Line

The Virage Logic ASAP Logic product line contains application-optimized libraries targeted to unique market requirements and is based on Virage Logic's proprietary and patented routing methodology and cell architecture. ASAP Logic Metal Programmable Cell Libraries are used in SoC designs to economically enable functional reprogrammability by changing only a few metal and via masks, and are often used as a design fabric for structured ASICs. ASAP Logic Standard Cell Libraries are optimized for area, speed, and power and provide up to a 30 percent increase in utilization when compared to conventional standard cell libraries.

About Synopsys HSPICE simulator

HSPICE simulator is the industry's "gold standard" for accurate circuit simulation and offers foundry certified MOS device models with state-of-the- art simulation and analysis algorithms. With over 25 years of successful design tape outs, HSPICE simulator is one of the industry's most trusted circuit simulator. HSPICE simulator is an integral component of Synopsys high-performance mixed-signal verification solution, Discovery AMS, which enables designers to achieve the highest throughput and accuracy for the largest mixed-signal SoC's. HSPICE simulator 2006.03, the latest HSPICE simulator version, comes with performance improvements for large extracted designs with sub 90 nm geometries. In addition, HSPICE simulator 2006.03 offers many new capabilities in the areas of Design for Yield, Signal Integrity, and RF design.

About Synopsys

Synopsys, Inc. is a world leader in EDA software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com .

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