Synopsys Design Compiler Topographical Technology Expedites ASIC Design at STMicroelectronics

Topographical Technology Eliminates Iterations Between STMicroelectronics and ASIC Customers to Reduce Turnaround Time

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that that STMicroelectronics (NYSE: STM), a leading supplier of semiconductors, has deployed Synopsys Design Compiler® topographical technology in its 90-nanometer (nm) and 65-nm application-specific integrated circuit (ASIC) design flow to expedite design time. STMicroelectronics is adopting Design Compiler topographical technology in its ASIC methodology to eliminate design iterations and streamline the overall design cycle for its internal design groups and for external customers.

In an ASIC model, reducing netlist iterations between the customer and ASIC vendor to achieve design closure is critical to completing a design on schedule. Design Compiler topographical technology accurately predicts final design timing, power, testability and area results prior to actual physical implementation, giving front-end designers early visibility into layout results. In this way, both the customer and ASIC vendor can be assured that the netlist generated after synthesis will, in fact, achieve the desired performance.

"Topographical technology offers much-needed predictability for a convergent RTL-to-GDSII path. Front-end designers no longer have to wait for layout results to uncover critical design issues; they can identify and fix them up front. In turn, back-end teams receive a better netlist for physical implementation which is more likely to meet the desired performance," said Philippe Magarshack, group vice president, Central CAD and Design Solutions, Front-End Technology Manufacturing, at STMicroelectronics. "We are extremely pleased with the results we have seen with topographical technology on advanced ASIC designs and have incorporated it in both our 90-nm and 65-nm ASIC design flows. We encourage our internal and external ASIC customers to use it for all their synthesis needs to expedite the design process."

Design Compiler topographical technology is an innovative, tapeout-proven synthesis technology that significantly reduces design time. It utilizes the Galaxy™ Design Platform physical implementation technologies to derive accurate interconnect delay data that allows the Design Compiler solution to predict post-layout design results such as timing, testability, and area during synthesis. In addition, topographical technology utilizes clock tree synthesis technology to estimate post-layout power results of the design, resulting in a highly predictable RTL-to-GDSII path.

"More and more market leaders like STMicroelectronics are recognizing the value of Synopsys topographical technology to help streamline their design flows and reduce design cycle time," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "We look forward to extending our collaboration with STMicroelectronics to support their ASIC customers through the broad deployment of topographical technology."

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

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