Synopsys Unveils Galaxy IC Compiler - Next-Generation Physical Design Solution

Leading-edge Customers Attest to Achieving Increased Performance and Productivity

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today unveiled Galaxy™ IC Compiler, the next-generation physical design solution, endorsed by leading-edge early users including Agere Systems, ARM and STMicroelectronics. IC Compiler transcends current-generation solutions by unifying previously separate operations. It is the first-ever physical design solution which provides concurrent physical synthesis, clock tree synthesis, routing, yield optimization and sign-off correlation, delivering unmatched design performance and productivity. IC Compiler is the centerpiece of the Synopsys Galaxy Design Platform, which provides a coherent solution from RTL to silicon.

"The innovations in IC Compiler represent our next-generation technology," said Aart de Geus, chairman and CEO of Synopsys. "This new architecture solves multiple design problems concurrently, bringing substantial productivity improvements in our customers' quality of results, time to results and cost of results. Early customers are already successfully applying this new technology to their toughest problems today."

"Designer productivity and out-of-the-box design performance are key concerns for ARM. IC Compiler has provided us considerably quicker time to results while hardening our synthesizable ARM® processor cores. Additionally, we have observed a marked improvement in maximum clock frequency achievable," said Keith Clarke, vice president of Engineering, ARM. "With its new TrueVue visualizer, comprehensive debug and analysis capabilities, and advanced optimizations, we think Synopsys has produced an excellent design solution."

The unrelenting march of technology coupled with the dynamics of a consumer-dominated market has created a situation where results and the cost of results are both important and interdependent. This dynamic requires a systemic solution, providing consistent optimization of timing, area, power, testability and yield across the flow from RTL down to silicon. Today, the Galaxy Design Platform is the designers' solution of choice. As technology challenges continue to multiply, leading-edge customers have collaborated with Synopsys to evolve the Galaxy Design Platform and develop IC Compiler as the key to performance and productivity in physical design.

"We value Synopsys as a key partner in the design automation field, and ST's strategy is to actively participate in new technology developments to shape the direction of products such as IC Compiler. This is part of our strategy to offer to our customers the best design capabilities on our latest technology platforms, such as our recently announced 65-nanometer platform," said Philippe Magarshack, group vice president, Central CAD and Design Solutions General Manager, STMicroelectronics. "With its single database, single timing engine, multi-mode capability, large capacity and next-generation architecture, we believe IC Compiler is very well-positioned to meet our needs for advanced physical implementation for our demanding SoC products in 65 and 45 nanometers."

IC Compiler provides high-quality results by harnessing the best of Synopsys' core technologies in synthesis, timing, placement, routing, lithography and sign-off, coupled with new innovations in physical design. Current-generation solutions integrate physical design steps into a single executable but have limited horizon because placement, clock tree synthesis and routing are separate, disjoint steps. Yield optimizations and timing signoff are also separate. IC Compiler unifies physical design by eliminating these separations through innovations in optimizations, yield enhancement and timing/SI signoff. A key innovation in IC Compiler is the XPS -- extended physical synthesis -- technology. XPS extends physical synthesis to full place and route, breaking down the walls between placement, clock tree and routing in current-generation solutions.

"We have been very impressed with the early results from IC Compiler," said Jon Fields, vice president with the Agere Systems Design Platform Organization. "We are planning to use the tool on the tapeout of a 90-nanometer production design. IC Compiler is proving to be key to making the difference where it counts the most -- smaller die-size, lower power dissipation and tight correlation with signoff."

Pricing and Availability

IC Compiler is expected to be available for production use starting in June 2005. List price for a full technology subscription license of IC Compiler for one year is $735,000. Licenses are available at lower annual rates for longer subscription terms, as are comprehensive upgrade paths for existing users of Synopsys physical

implementation technology.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California and has offices in more than 60 locations throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/ .

Forward Looking Statements

This press release contains forward-looking statements within the meaning of the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits and dates of availability of the Galaxy IC Compiler design solution. These statements are based on Synopsys' current expectations and beliefs. Actual results could differ materially from the results implied by these statements as a result of unforeseen difficulties in finalizing the production release of the solution, uncertainties attendant to any new product offering and the other factors contained in Synopsys' Quarterly Report on Form 10-Q for the fiscal quarter ended January 31, 2004.

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SOURCE: Synopsys, Inc.

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