# STARC Adopts IC Compiler to Boost Efficiency of Production Flow

## Enhanced STARCAD-21 RTL-to-GDSII Production Flow Ready for Deployment at Major Japanese Semiconductor Companies

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Synopsys Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that the Semiconductor Technology Academic Research Center (STARC) has adopted IC Compiler, Synopsys' next-generation place-and-route solution, in its newly released STARCAD-21 V3.0 production flow. STARC is an influential consortium of Japan's major semiconductor manufacturers that is seen as leading the way on advanced design methodologies in Japan. It provides its members a comprehensive RTL-to-GDSII design methodology called STARCAD-21 that incorporates the latest tools, libraries, and flows for 90-nanometer and below system-on-chip (SoC) design. STARC's goals for this release of STARCAD-21 were to reduce design margins and to improve the efficiency of the RTL-to-GDSII flow. STARC incorporated IC Compiler into the STARCAD-21 flow because it provides up to 2X faster run times and better quality of results (QoR) compared to the previous-generation STARCAD-21 flow.

"Synopsys had very impressive projections when they first introduced us to IC Compiler," said Nobuyuki Nishiguchi, vice president of the Design Methodology Group at STARC. "We are happy to confirm that IC Compiler has indeed delivered 2X faster run times, better QoR, and smaller area for high-performance designs. This new release of STARCAD-21 with support for IC Compiler represents a big step forward for our member companies in achieving high designer productivity."

STARC has invested months of intensive effort to build the new STARCAD-21 flow and to thoroughly evaluate all its elements. It delivered to its 11 members a flow with increased designer productivity that also supports a range of advanced capabilities in test, hierarchy, clock planning and low-power design. To achieve these goals, STARC adopted not only IC Compiler, but also DFT MAX for test compression and Synopsys' new high-accuracy CCS library format. CCS library models allowed STARC to reduce the design margin for on-chip variation by 5% and boosted productivity by providing a 50X speed-up in the development of noise libraries.

IC Compiler's unique Extended Physical Synthesis (XPS) technology enables the STARCAD-21 flow to efficiently deal with increasingly common multi-mode designs. IC Compiler's concurrent multi-mode capability was the key to significant improvements in performance and turnaround time. For example, a RISC core with six operating modes and two process corners was concurrently optimized across all modes by IC Compiler. Thanks to XPS' true concurrent optimization for timing and area, there was a 5X improvement in turnaround time for post-detail routing optimization. Further efficiency gains were measured in STARCAD-21 resulting from the excellent correlation of IC Compiler to PrimeTime® SI sign-off timing and the simplified Tcl scripting.

"We are already seeing very strong momentum with IC Compiler in Japan," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "As major Japanese design houses are closely following developments at STARC, STARCAD-21 V3.0 featuring IC Compiler is an added boost. We look forward to working closely with customers to help them realize the productivity gains validated by STARC."

About IC Compiler

IC Compiler is Synopsys' next-generation place-and-route system. It provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure. Current-generation solutions have a limited horizon because placement, clock tree, and routing are separate, disjointed operations. IC Compiler's Extended Physical Synthesis (XPS) technology breaks down the walls between these steps by extending physical synthesis to full place-and-route. IC Compiler has a unified, TCL-based architecture that implements innovations and harnesses some of the best Synopsys core technologies. It is a complete place-and-route system with everything necessary to do next-generation designs, including physical synthesis, placement, routing, timing, signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.



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