Latest Release of Synopsys IC Compiler Delivers Faster Design Closure

New Advances Include Faster Performance, Top-level Closure and DRC Repair

MOUNTAIN VIEW, Calif., Jan. 31, 2011 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the availability of the latest release of IC Compiler, a key component of the Galaxy™ Implementation Platform. This development caps a year of leading innovations in physical design productivity. For two years in a row, IC Compiler has won an EDN Innovation Award. In 2010 it won for In-Design Physical Verification. The IC Compiler 2010.12 release advances this capability, making automatic DRC repair up to 7X faster. This latest release also delivers new performance improvements for multicorner/multimode (MCMM) designs bringing the total for the year to a nearly 4X speed-up. Additionally, IC Compiler 2010.12 introduces technology specifically targeted for final top-level design closure, helping accelerate turnaround-time by 2X to 3X. Finally, IC Compiler 2010.12 delivers quality-of-results (QoR) improvements, focusing on power reduction.

"With our 28 nanometer Stratix® V FPGAs, we have pushed the boundaries of performance, density and integration," said Brad Howe, vice president of IC engineering at Altera Corporation. "IC Compiler's key technologies such as concurrent multicorner/multimode (MCMM) optimization and In-Design automatic DRC repair were a strong enabler for us to achieve our performance and area targets, allowing us to meet our tight design schedule."

Power-sensitive designers have access to a powerful leakage optimization engine integrated in IC Compiler. Recommended for final-stage leakage recovery on a close-to-tapeout design, this engine is architected to deal with a multitude of cell variants to deliver optimal leakage reduction while preserving timing. This release also delivers up to 10 percent lower out-of-the-box clock tree power and a 10 percent reduction in total buffer count for reduced dynamic power consumption. Additional QoR improvements include advances in clock feasibility, signal integrity and electro-migration closure.

The IC Compiler 2010.12 release continues to improve runtime performance, delivering an additional 1.5X speed-up along with a 20 percent reduction in memory. On-Demand Loading technology (ODL), first introduced to significantly reduce time-to-floorplan creation, has been extended to top-level closure to accelerate turnaround-time by 2X to 3X. Using ODL, concurrent optimization of top and block interfaces enables blocks to be adjusted transparently, reducing the need for costly feedback loops between top-level and block-level implementation. IC Compiler In-Design physical verification technology dramatically reduces design iterations by enabling signoff-accurate DRC analysis and repair during design. In this release, incremental revalidation of repair regions and improved fix rates result in up to 7X faster automatic DRC repair times.

"The latest IC Compiler release demonstrates our strong focus on technology innovation that delivers compelling customer value," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "In the high-end FPGA market where time to market is a key differentiator, IC Compiler In-Design technology has successfully addressed one of Altera's key design productivity concerns."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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