Agere Systems Accelerates Tapeout of High-Performance SOC with Synopsys IC Compiler

IC Compiler Fits Easily in the Agere Flow, Delivers Higher Performance

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Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that Agere Systems Inc. has used Synopsys' IC Compiler next- generation place-and-route system to tape out a 90-nanometer (nm) multi-core DSP system-on-chip (SoC) for telecom applications. The Agere design team needed to reduce routing congestion on this SoC while meeting timing and power specifications. IC Compiler fit easily into the Agere flow and delivered initial results in just two days. Agere's final results with IC Compiler were completed in less time and showed significantly improved routability and higher performance.

"We were able to easily deploy IC Compiler and produced better results than we could achieve before," said Jill Bennett, engineering director with Agere's Telecommunications Division. "We are encouraged by these excellent results, and are now pursuing IC Compiler deployment across multiple designs."

The new Extended Physical Synthesis (XPS) architecture in IC Compiler -- combined with the tool's multi-threshold capabilities -- enabled Agere to concurrently optimize for timing and power, reducing routing congestion and speeding the time to closure.

"Agere's tapeout success underscores Synopsys' commitment to help customers reduce their time-to-market and deliver chips with higher performance and yield," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "We look forward to working closely with customers like Agere to enable their full use of IC Compiler to achieve higher performance and productivity for competitive advantage."

About IC Compiler

IC Compiler is Synopsys' next-generation place-and-route system. It provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure. Current generation solutions have a limited horizon because placement, clock tree and routing are separate, disjointed steps. IC Compiler's Extended Physical Synthesis (XPS) technology breaks down these walls by extending physical synthesis to full place-and-route between these steps through a unified, TCL-based architecture that implements innovations in optimization as well as harnessing the best of Synopsys' core technologies in physical synthesis, placement, routing, timing and signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization.

About Synopsys

Synopsys, Inc. is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at www.synopsys.com.

Editorial Contacts:

Nancy Renzullo
Synopsys, Inc.
(650) 584-1669
renzullo@synopsys.com

Angela Costa
Edelman Public Relations
(650) 429-2765
Angela.Costa@edelman.com

SOURCE: Synopsys, Inc.

CONTACT: Nancy Renzullo of Synopsys, Inc., +1-650-584-1669, or
renzullo@synopsys.com; or Angela Costa of Edelman Public Relations,
+1-650-429-2765, or Angela.Costa@edelman.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/