Synopsys and TSMC Deliver 3D-IC Design Support

Design Tools Selected in TSMC's First Integrated, Validated Reference Flow and Design Kit Enabling Multi-Die Integration Using TSMC CoWoS Technology

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Highlights:

- Supports multi-die integration using TSMC CoWoS™ technology
- Includes enhanced versions of Synopsys' Galaxy™ Implementation Platform tools
- Increases productivity, accelerates time to market and speeds time to volume

Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that it is delivering a comprehensive 3D-IC design solution that is included in TSMC's CoWoS™ (Chip on Wafer on Substrate) Reference Flow. The design flow is the result of the latest collaboration between the companies on 3D-IC integration technologies. It provides a smooth transition from a traditional "2D" integrated circuit (IC) to a multi-die stacking design flow. In support of the TSMC CoWoS reference flow, Synopsys has released enhanced versions of its Galaxy Implementation Platform tools for physical implementation, parasitic extraction, physical verification and timing analysis With the new flow and tool enhancements, engineers can increase productivity, shorten time-to-market and speed time-to-volume when designing multi-die systems for TSMC CoWoS silicon.

"3D-IC integration technologies offer tangible benefits for design teams looking to deliver extreme performance, the smallest form factor, and the lowest power consumption," said John Chilton, senior vice president of marketing and corporate development at Synopsys. "3D-IC integration is proving to be key to extending the lifespan of established semiconductor processes and enabling the integration of heterogeneous technologies, complementing traditional 'Moore's Law' transistor scaling for many application domains. Synopsys' contributions to the TSMC CoWoS Reference Flow enable designers to quickly realize innovative and advanced multi-die systems."

"TSMC and Synopsys have a long-term collaboration on design flows," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "The combination of Synopsys EDA tools with TSMC CoWoS technology provides designers with a productive answer for manufacturability of multi-die systems that optimize performance and power consumption."

Synopsys' Galaxy Implementation Platform features support for TSMC's CoWoS reference flow and technology. TSMC has validated Synopsys' implementation, analysis and signoff tools, including:

Physical Implementation

- IC Compiler™ multi-die physical implementation with support for placement, assignment and routing of microbump, thru-silicon via (TSV), probe-pad and C4; combo bump cells allowing simplified and flexible bump assignment; microbump alignment checks; redistribution layer (RDL) and signal routing, and power mesh creation on CoWoS interconnection layers

Analysis and Signoff

- Hercules layout vs. schematic (LVS) connectivity checking between stacked die
- StarRC™ Ultra parasitic extraction support for TSV, microbump, RDL and signal routing metal for CoWoS design interconnection
- PrimeTime® timing analysis of multi-die systems

Synopsys' 3D-IC solution is currently in limited customer availability. For more information on the Synopsys 3D-IC solution, please visit: www.synopsys.com/3D-IC.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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