Synopsys Extends Support for ARM AMBA Protocol Verification with New Performance Checker for AMBA 4 AXI4

Next-generation Discovery Verification IP Enables Identification and Debug of SoC Performance Bottlenecks

MOUNTAIN VIEW, Calif., Oct. 29, 2012 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, today announced that its next-generation Discovery™ Verification IP (VIP) for the ARM® AMBA® 4 AXI4™ protocol now offers a Performance Checker capability. This capability enables system-on-chip (SoC) verification teams to analyze and validate SoC performance using metrics established during the system architecture definition process, speeding up the debug of SoC performance bottlenecks.

"Developing high-performance products quickly and predictably is critical for the SoC market. With increased SoC complexity, the integration of multiple blocks frequently produces performance bottlenecks that need to be examined and eliminated," said Joe Convey, director of design enablement, ARM. "The Performance Checker capability in Synopsys' Discovery VIP for AMBA 4 AXI4 offers an innovative approach that leverages the investment made in optimizing the system architecture to SoC verification, accelerating the overall verification process."

The Performance Checker capability builds on Discovery VIP data integrity checking to track latencies across an AMBA 4 AXI4 or ACE™ interconnect. Metrics defined in Synopsys' Platform Architect™ during architecture exploration are passed to the Discovery VIP as constraints to ensure consistency of system-performance through the design flow. The Performance Checker capability then enables the Discovery VIP to identify performance violations and generates reports that help users validate their implementation against the optimized system's performance goals, with a substantially wider range of real-life traffic. Additionally, violations are highlighted in Synopsys' Protocol Analyzer protocol-aware debug environment to simplify debug and accelerate root-cause analysis.

"The ARM AMBA protocols continue to facilitate the development of high-performance multi-processor SoCs," said Debashis Chowdhury, vice president of R&D for the Synopsys Verification Group. "With the introduction of the Performance Checker capability in our Discovery VIP, we continue our focus on addressing SoC verification requirements and help improve the productivity of teams using the AMBA protocols to meet their SoC performance goals."

The Synopsys Discovery VIP Performance Checker as well as the rest of the Synopsys verification and implementation solutions for the design of ARM Powered® SoCs will be on display all three days of the 2012 ARM TechCon Expo, October 30 – November 1, 2012. To learn more about what Synopsys will be discussing during their multiple conference sessions, please visit http://www.synopsys.com/Community/Partners/ARM/Pages/ARMTechnologyConference2012.aspx

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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