Synopsys Announces Adoption of its TetraMAX ATPG and Yield Explorer Tools by STMicroelectronics as Essential Enablers of Rapid Yield Ramp

Design-centric Volume Diagnostics Accelerate Identification of Systematic Failure Mechanisms

MOUNTAIN VIEW, Calif., Nov. 5, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq:SNPS), a global leader accelerating innovation in the design, verification and manufacture of chips and systems, today announced that STMicroelectronics (ST) has adopted Synopsys' volume diagnostics solution company-wide for faster yield ramp. IC product teams must rapidly isolate and correct systematic failure mechanisms to ramp up new IC designs from low initial yield to mature yield in volume production. Synopsys' solution has enabled ST engineers to quickly identify the most dominant systematic failure mechanisms on new designs, thereby driving yield improvement at a faster rate.

The solution is comprised of two integrated products from Synopsys: the TetraMAX[®] ATPG and Yield Explorer® tools. TetraMAX ATPG provides physical diagnostics that enable the localization of defects on chips that fail logic scan tests. Yield Explorer analyzes the defect locations from multiple failing chips and correlates them with design data to prioritize systematic yield issues and guide physical failure analysis. Integration of TetraMAX ATPG and Yield Explorer into ST volume diagnosis flow has enabled ST to dramatically shorten root cause analysis time and achieve rapid yield ramp on new designs.

"Recognizing that subtle systematic failures are critical to yield ramp at nanometer process nodes, we collaborated with Synopsys to bring design, test and manufacturing data together in volume diagnostics," said Roberto Mattiuzzo, SoC Test and Diagnosis manager at STMicroelectronics' Central CAD and Design Solutions. "Highly accurate physical diagnostics from TetraMAX ATPG and Yield Explorer's design-centric data analysis and correlation capabilities have allowed us to perform faster failure analysis and fab process tuning. Among other benefits, this has resulted in significant improvements in root cause isolation effectiveness hence leading to yield improvements across multiple products/technologies."

The Synopsys volume diagnostics solution offers detailed engineering analyses as well as automated production analysis and reporting. Expert users benefit from the flexibility to bring design, fab and test data together and analyze these with an exploratory approach. Time-sensitive production teams rely on automated analysis routines to create various reports and provide a quick first view of yield issues on new production batches. The integrated solution is simple to deploy and offers a unified interface for physical design and tester output data for higher efficiency.

"Yield Explorer easily accommodates the wide variety of yield analysis requirements across our business units and is fully customizable to suit their range of data types, analysis and reporting preferences," said Andrea Burri, Supply Chain Solutions director at STMicroelectronics' Company Central Planning. "In addition to being deployed for volume diagnostics, Yield Explorer will be used by product engineers across ST to perform traditional yield analyses based on functional, parametric and embedded memory tests."

"Systematic yield loss due to design-process interactions requires complex analyses incorporating many different types of design data," said Howard Ko, senior vice president and general manager of the Silicon Engineering Group at Synopsys. "ST is a pioneer in recognizing volume diagnostics as the most effective method to bring design data into yield analysis. ST and Synopsys have collaborated in refining the Yield Explorer usage and TetraMAX ATPG diagnostics during all phases of new product yield ramp so that design and product engineers may easily use it across a wide range of products."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

Editorial Contacts:

Tess Cahayag Synopsys, Inc. 650-584-5446 maritess@synopsys.com Lisa Gillette-Martin MCA, Inc. 650-968-8900 ext. 115 lgmartin@mcapr.com

SOURCE Synopsys, Inc.