Synopsys Extends Mobile Storage Leadership with UFS and MIPI Alliance UniPro Controller IP

New DesignWare UniPro Controller IP Streamlines Development of Storage, Camera and Display Interfaces

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Highlights:

- Comprehensive mobile storage solution supporting new JEDEC UFS v1.1 interface standard includes Synopsys' DesignWare® MIPI® UniPro℠ and Universal Flash Storage (UFS) Controllers and DesignWare MIPI M-PHY
- Highly configurable DesignWare MIPI UniPro controller enables area- and feature-optimized host and device implementations for mobile storage (UFS), camera (MIPI CSI-3) and future display (MIPI DSI-2) SoCs
- Single-vendor UniPro IP platform simplifies integration and reduces implementation risk

Synopsys, Inc. (Nasdaq:SNPS), a global leader accelerating innovation in the design, verification and manufacture of chips and systems, today announced the availability of the DesignWare MIPI UniPro Controller for host and device storage, camera and display applications, and the DesignWare UFS Host Controller for storage applications. The new IP works in tandem with the multi-gear DesignWare MIPI M-PHY IP to accelerate the implementation of the MIPI Alliance UniPro and UFS interface standards in application processors, mobile systems-on-chips (SoCs) and peripheral ICs.

(Photo: http://photos.prnewswire.com/prnh/20120924/AQ79282-INFO)

The DesignWare UFS Host Controller complies with the JEDEC UFS v1.1 standard and integrates both a MIPI UniPro controller and a UFS host application layer. In this configuration, the UniPro Controller is pre-configured for UFS host implementation to provide an area- and feature-optimized solution. The UFS host application layer manages the UFS protocol between the host and an external UFS device. The UFS Controller can be used with the multi-gear DesignWare MIPI M-PHY IP for a comprehensive, future-proof, mobile storage interface that unifies all non-volatile interfaces within a mobile device.

"Synopsys' release of UFS Controller IP demonstrates the fast adoption of the UFS standard that we're seeing in the mobile industry," said Mian Quddus, Chairman of the JEDEC Board of Directors and the JC-64 Committee for Embedded Memory Storage and Removable Memory Cards. "By delivering this mobile storage product based on JEDEC UFS, Synopsys is helping to enable higher data throughput compared to existing mobile storage interfaces."

The DesignWare MIPI UniPro Controller can be application-optimized for all UniPro-based host and device implementations (UFS, CSI-3 and DSI-2) because of its extensive configurability options, including traffic classes, test features, data widths and receive and transmit lanes to the M-PHY. The UniPro Controller, compliant with the MIPI UniPro v1.41 specification, connects to the application layer with write and read C-port interfaces, a configuration interface to program all layers, and a MIPI Alliance M-PHY® adaptation layer supporting the Reference M-PHY Module Interface (RMMI).

"IP supporting the MIPI UniPro v1.41 specification gives designers the ability to rapidly build host and device configurations into their mobile storage SoCs," said Joel Huloux, MIPI Alliance Chairman. "Synopsys' introduction of their DesignWare MIPI UniPro Controller promotes a robust MIPI ecosystem while furthering the development and reach of the latest MIPI specifications."

"Combined with the recent release of our multi-gear MIPI M-PHY IP, the DesignWare UFS Host Controller gives SoC designers a quick and reliable path for JEDEC UFS adoption that helps ensure system-level interoperability and increases the likelihood of first-time-right silicon success," said John Koeter, vice president of marketing for IP and systems at Synopsys. "In addition, our new, highly configurable MIPI UniPro Controller IP services all UniPro-based protocols, giving designers a flexible UniPro IP solution that reduces integration effort and risk."

Availability

The DesignWare MIPI UniPro Controller IP, UFS Host Controller IP and M-PHY IP are available now.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad

DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware/software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier compared to traditional methods. With a robust IP development methodology, extensive investment in quality, IP prototyping, software development and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) accelerates innovation in the global electronics market. As a leader in electronic design automation (EDA) and semiconductor IP, its software, IP and services help engineers address their design, verification, system and manufacturing challenges. Since 1986, engineers around the world have been using Synopsys technology to design and create billions of chips and systems. Learn more at www.synopsys.com.

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