Latest Release of Synopsys IC Validator Delivers Faster Manufacturing Compliance For 20nm and Below

Advances Include Faster Runtime, ECO Flows and New Process Modeling Technology

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Highlights:

- Qualified by leading foundries for 20 nanometers (nm)
- Successful in numerous tapeouts targeted for 20nm
- Introduces new double patterning (DPT) decomposition checking and pattern matching technologies for optimal compliance with foundry manufacturing requirements
- Enables reduced verification turnaround time with demonstrated scalability to 64 cores and beyond
- Expands In-Design technology for automatic DRC/DPT repair and 2X faster ECOs

Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced the release of IC Validator 2012.06, Synopsys' physical verification platform for advanced process nodes. With immediate availability of qualified rule decks by leading foundries, IC Validator 2012.06 offers new technologies that enable physical signoff verification at advanced process nodes. IC Validator 2012.06 continues to build on Synopsys' approach of speeding design closure through In-Design physical verification with Synopsys' IC Compiler™ place and route solution, enabling place-and-route engineers to eliminate late stage surprises and manual repairs. New additions to the In-Design flow, targeted for 20nm and below, include DPT and pattern matching technology. This latest release of IC Validator also offers a significant performance boost for verifying large and complex 20-nm designs. By maximizing the utilization of mainstream computing hardware through innovative techniques, IC Validator can enable engineers to parallelize design rule checks (DRCs) on 64 processing cores and beyond, thereby significantly reducing verification turnaround time for these advanced process nodes.

"To address the complexities of 20nm process, we are actively expanding the use of In-Design Physical verification with IC Compiler and IC Validator for our new designs," said Kyu-Myung Choi, senior vice president of Infrastructure Design Center, Samsung Electronics.

Enabling Physical Verification at 20nm and Below
To address the stringent manufacturing requirements of 20-nm design, IC Validator 2012.06 introduces several new advances in process modeling technology:

- **Double Patterning:** The limitations of current lithographic technology require layout to be split into two masks of alternating structures. IC Validator features a fast and accurate, native decomposition ("coloring") engine. IC Validator can perform decomposition checks during design and can also drive automatic fixing of violations with IC Compiler via the In-Design technology. IC Validator can also perform the final signoff quality check alongside the final design rule check.
- **Pattern Matching:** Occasionally layout patterns can generate lithography hotspots, leading to accidental open or short connections. IC Validator's patented pattern-matching technology augments DRC with intuitive 2D multi-shape pattern analysis for ultra-fast detection of manufacturing hotspots. It can also drive automatic fixing of these hotspots with IC Compiler. Leading manufacturers will thus be able to achieve better process margins and higher yields for the 20-nm process node.

Improving Design Turnaround Time
IC Validator is being broadly used by design teams for In-Design physical verification with IC Compiler. This release complements IC Compiler 2012.06, allowing users to benefit from 2X faster ECO and automatic design repair (ADR) flows. New additions to In-Design technology also make it possible for designers to perform layout enhancement for yield natively within IC Compiler, streamlining the design flow and eliminating wasteful iterations.

In addition to being used for In-Design verification, IC Validator is also fully qualified for physical signoff at leading foundries across a broad range of process technologies. IC Validator 2012.06 deploys a range of distributed multiprocessing techniques to achieve optimal utilization of available hardware. These technologies, including multi-threading, on-demand load balancing and memory-aware scheduling, have demonstrated scalability to 64 cores and beyond. With this release, customers designing at advanced process nodes can now benefit from a significant productivity boost and faster turnaround times.

"IC Validator 2012.06 is the most noteworthy release for our physical verification product line to date," said Antun Domic, senior vice president and general manager of Synopsys' implementation group. "Beyond

enabling verification of the highly complex 20-nanometer process technology node at Samsung and other leading foundries with a multitude of new technologies, we have added significant improvements in runtime, scalability and In-Design productivity that will benefit our entire customer base."

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

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