Synopsys Launches Industry's First Integrated Hybrid Prototyping Solution

Out-of-the-Box Solution Seamlessly Integrates Virtualizer™ Virtual Prototyping and HAPS® FPGA-Based Prototyping to Accelerate SoC Software and Hardware Development

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Highlights:

- Get the best of both worlds with a hybrid prototype that seamlessly links virtual and FPGA-based prototypes
- Start multi-core SoC prototyping earlier and achieve high-performance execution of system-level models with directly connected real-world hardware interfaces
- Partition SoC design blocks between virtual and FPGA-based prototype environments to maximize overall prototype performance
- Accelerate system bring-up by using virtual prototyping for new design blocks and FPGA-based prototyping for existing logic
- Improve debug visibility and control of software under development through the Virtualizer-based environment
- Easily integrate high-performance ARM® Cortex™ processor models, transactors for ARM AMBA® interconnect and Synopsys® DesignWare® IP with the rest of your design into a single hybrid prototype

Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced an integrated hybrid prototyping solution that combines Synopsys' Virtualizer virtual prototyping and Synopsys' HAPS FPGA-based prototyping to accelerate the development of system-on-chip (SoC) hardware and software. By using Virtualizer virtual prototyping for new design functions and HAPS FPGA-based prototyping for reused logic, designers can start software development up to 12 months earlier in the design cycle. In addition, Synopsys' hybrid prototyping solution enables designers to accelerate hardware/software integration and system validation, significantly reducing the overall product design cycle. With high-performance models for ARM Cortex processors, ARM AMBA protocol-based transactors, and DesignWare IP, developers can easily partition their ARM processor-based designs into virtual and FPGA-based prototypes as best suited to their design requirements.

Today, designers use two relatively independent methods for SoC prototyping: transaction-level model (TLM)-based virtual prototyping and FPGA-based prototyping. Virtual prototyping is ideal for accelerating pre-RTL software development by executing fast TLMs and provides more efficient debug and analysis scenarios. FPGA-based prototyping provides cycle-accurate, high-performance execution and direct real-world interface connectivity. Synopsys' hybrid prototyping solution blends the strengths of both Virtualizer virtual and HAPS FPGA-based prototyping to enable software development and system integration much sooner in the project lifecycle.

"The rising complexity and software content associated with multi-core SoCs means that system engineers and software developers cannot wait for hardware to begin their work; so, they are increasingly utilizing prototypes of their chips and systems," said Chris Rommel, vice president, embedded software and hardware, of VDC Research. "Synopsys' 'hybrid' approach addresses many of the limitations of standalone SoC prototyping methods by allowing developers to freely mix pre-RTL transaction-level models with RTL that already exists or is being created, giving design teams a significant head start on their hardware and software development."

Synopsys' hybrid prototyping solution enhances software stack validation through very high-speed execution of processors using a Virtualizer virtual prototype. It allows direct connection to real-world I/O model interfaces through analog PHYs or test equipment attached to a HAPS FPGA-based prototype. In addition, designers can take advantage of existing RTL or IP in the FPGA-based prototype and new functions in SystemC transaction-level models, which are faster to implement and available much sooner in a project lifecycle.

Synopsys' high-performance HAPS Universal Multi-Resource Bus (UMRBus) physical link efficiently transfers data between the virtual and FPGA-based prototyping environments. The pre-verified HAPS-based transactors, supporting ARM AMBA 2.0 AHB™/APB™, AXI3™, AXI-4™ and AXI4-Lite™ interconnects, give designers the flexibility to partition the SoC design between the virtual or FPGA-based prototyping environments at the natural block-level boundaries of the AMBA interconnect. By using the software debug capability within the Virtualizer-based environment in a hybrid prototype, users have greater visibility and control into the register and memory files of the software under development compared to traditional FPGA-based prototyping.

"Hybrid prototyping offers design teams the best of what both hardware and software prototyping have to

offer," said John Koeter, vice president of marketing for IP and systems at Synopsys. "By integrating the strengths of Virtualizer virtual prototyping with HAPS FPGA-based prototyping using the UMRBus physical link, Synopsys enables designers to develop fully operational SoC prototypes much faster and earlier in the design cycle, and accelerate software development and full system validation."

Availability
The hybrid prototyping solution is available now to early adopters.

Hybrid Prototyping at DAC 2012
Synopsys will be demonstrating the integrated hybrid prototyping solution at DAC 2012, booth #1130. DAC takes place in San Francisco, CA June 3 – 7, 2012. For more information on Synopsys' participation at DAC 2012 visit www.synopsys.com/dac.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

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