Synopsys' StarRC Extraction Solution Certified by UMC for 28-nm Designs

StarRC Technology Files Silicon-Validated and Available to UMC's 28-nm Customers

MOUNTAIN VIEW, Calif., April 3, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that UMC has certified Synopsys' StarRC™ parasitic extraction solution for its latest 28-nanometer (nm) process technologies. The StarRC solution delivered silicon-validated accuracy on UMC's evaluation designs to meet the qualification criteria for its advanced 28-nm Poly SiON and High K/Metal gate processes. The StarRC technology files are immediately available to UMC customers working with its 28-nm processes.

"UMC has continued to work with leading EDA companies such as Synopsys to make available to its customers high-quality solutions that pave the way to silicon success," said S. C. Chien, vice president of Customer Engineering & IP Development Design Support Divisions at UMC. "The qualification of Synopsys' proven StarRC parasitic extraction solution for UMC's 28-nanometer process technology strengthens the portfolio of resources available to our customers for 28-nanometer designs. Mutual customers can now take full advantage of our latest foundry processes and successfully bring their innovations to the marketplace."

StarRC is a key component of Synopsys' Galaxy™ Implementation Platform and the industry-leading parasitic extraction solution for system-on-chip (SoC), custom digital, analog/mixed-signal (AMS) and memory designs. StarRC's 28-nm features include modeling for key parasitic effects, including advanced retargeting effects, new via etch and coupling effects, area-dependent via resistance and capacitance, polynomial-based diffusion resistance, and enhanced layout-dependent device parasitic extraction. StarRC also offers other advanced capabilities for 28-nm designs, including unified Rapid3D technology for fast, high-accuracy 3D extraction, enhanced multicore performance and scalability, proprietary reduction capabilities and the smallest netlist for signoff of the largest SoC designs.

"StarRC continues to lead the industry in use for parasitic extraction and signoff of advanced node designs," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "UMC's validation of StarRC extends the benefits of our state-of-the-art process modeling and extraction technology to UMC's 28-nanometer customers, enabling them to deliver their high-performance 28-nanometer devices to market with increased confidence."

About Synopsys®

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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