Synopsys, Altera and TSMC Collaborate to Deliver Silicon-Accurate Parasitic Modeling and Extraction for 28-nm Processes

Altera Deploys Synopsys' StarRC Extraction Solution to Accelerate Time to Market for 28-nm FPGA Designs

MOUNTAIN VIEW, Calif., March 28, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that it collaborated with Altera and TSMC to silicon-validate modeling of key parasitic effects in Synopsys' StarRC™ solution for TSMC's 28-nanometer (nm) processes. The StarRC solution achieved the stringent model-to-silicon accuracy criteria of TSMC's 28-nm process technology to enable high-performance designs at the advanced node. Altera Corporation, a pioneer in programmable logic, has successfully deployed StarRC to achieve signoff accurate extraction and accelerate the design cycle of its 28-nm FPGA designs.

"We have trusted StarRC as a standard parasitic extraction solution to realize our aggressive design and signoff analysis goals at the 40-nanometer node and above," said Eugene Chen, director of CAD engineering at Altera Corporation. "Our 28-nanometer collaboration demonstrated that StarRC continues to meet the rigorous accuracy and performance criteria we employ for tool selection to deliver high-quality products to our customers. StarRC is now fully deployed as the signoff parasitic extraction solution for our most advanced 28-nanometer Stratix V FPGA devices in production."

At advanced nodes (28-nm and below), process modeling complexity has increased significantly due to continued transistor scaling, the increasing number of metal and dielectric layers, new device structures and the increased field effects between devices and interconnects. Several second-order effects that could be ignored in the past must now be accurately modeled and extracted to ensure desired circuit behavior. StarRC offers silicon-accurate modeling for the new 28-nm process effects as validated by foundries and customers on their taped-out designs. StarRC's key 28-nm features include: modeling of increased conductor width variation due to advanced retargeting and optical-proximity-correction (OPC) effects, via-faceting and coupling effects of larger via shapes; area-dependent via resistance and capacitance; and enhanced layout-dependent device parasitic extraction. In addition, the StarRC solution includes the Rapid3D field solver technology for fast, high-accuracy 3D extraction that is also qualified by TSMC for the 28-nm node.

"We have collaborated closely with Synopsys through several generations of process nodes to accurately model complex parasitic effects and qualify StarRC for TSMC's advanced process technologies including 28-nanometer," said Suk Lee, senior director of design infrastructure marketing at TSMC. "We are pleased to see our mutual customers, such as Altera, realize the benefits of this collaboration and deploy the solution to achieve a high standard of accuracy on their leading-edge 28-nanometer designs."

"Synopsys continues to collaborate with TSMC and Altera to ensure accurate parasitic modeling by our proven StarRC extraction solution and deliver technology for silicon success of next-generation designs," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Altera's successful tapeout of Stratix V FPGAs demonstrates the success of our continued investment in StarRC's high-performance extraction technology."

About Synopsys®

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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