Synopsys' StarRC Extraction Solution Enables More Than 150 Successful 28nm Tapeouts

Qualified by More Than 40 Leading Semiconductor Companies, StarRC Extraction Solution Achieves the Industry's Broadest 28nm Usage

MOUNTAIN VIEW, Calif., March 28, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP used in the design, verification and manufacture of electronic components and systems, today announced that its StarRC™ parasitic extraction solution has enabled more than 150 successful 28-nanometer (nm) tapeouts, delivering fast turnaround time and the signoff accuracy required for next-generation designs across computer, consumer, mobile and wireless communications applications. StarRC's advanced modeling of complex process effects at the 28-nm silicon process technology node and its leading qualification by major foundries provides lower design risk and improved opportunity for one-pass tapeout success. StarRC is already used by more than 40 semiconductor companies for 28-nm design signoff, confirming its position as the industry's gold standard extraction solution through several generations of process technologies.

Companies that have qualified and selected the StarRC solution for use in their 28-nm signoff and tapeout flows include Altera Corporation, Bull, Fujitsu Semiconductor, HiSilicon Technologies, Imagination Technologies, LSI Corporation, Moortec Semiconductor, NVIDIA, Qualcomm Incorporated, Renesas Electronics Corporation, Samsung, STMicroelectronics, Toshiba and others.

"Delivering an extraction solution that enables our customers to achieve their aggressive signoff goals with confidence is a critical priority at each new process node," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Crossing the 150-tapeout milestone at 28 nanometers is a strong validation of StarRC's strengths and our continued collaboration with foundries. It is also an excellent testimony to the broad range of customer designs benefitting from its capabilities."

About StarRC
StarRC is a key component of Synopsys' Galaxy™ Implementation Platform and the leading parasitic extraction solution for system-on-chip (SoC), custom digital, analog/ mixed-signal (AMS) and memory designs. StarRC's 28-nm features include advanced modeling for new interconnect and device parasitic effects. These capabilities were developed and validated in close collaboration with major silicon foundries and other leading-edge customers, helping to ensure the best model-to-silicon correlation. To improve productivity, StarRC also offers unified Rapid3D fast field solver, enhanced multicore technology with adaptive extraction algorithms and proprietary reduction capabilities for faster extraction, and the smallest netlist to sign-off for the largest 28-nm SoC designs.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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