Synopsys Unveils 3D-IC Initiative

Comprehensive EDA Solution to Enable Design of Stacked Multi-Die Systems Using TSV and Silicon Interposer Technologies

MOUNTAIN VIEW, Calif., March 26, 2012 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today unveiled its initiative to accelerate the design of stacked multiple-die silicon systems using 3D-IC integration to meet the requirements of faster and smaller electronic products that consume less power. As part of its 3D-IC initiative, Synopsys is working closely with leading IC design and manufacturing companies to deliver a comprehensive EDA solution, including enhanced versions of its IC implementation and circuit simulation products.

3D-IC technology complements conventional transistor scaling to enable designers to achieve higher levels of integration by allowing multiple die to be stacked vertically, or in a side-by-side "2.5D" configuration on a silicon interposer. 3D-IC integration uses through-silicon via (TSV) technology, an emerging interconnection technology that will replace the traditional wire-bonding process in chip/wafer stacking. The use of TSVs can increase inter-die communication bandwidth, reduce form factor and lower power consumption of stacked multi-die systems.

"As 2D scaling becomes impractical, 3D-IC integration becomes the natural evolution of semiconductor technology; it is the convergence of performance, power and functionality," said Phil Marcoux, managing director at PPM Associates. "Some of the benefits of 3D-IC integration, such as increasing complexity, improved performance, reducing power consumption and decreasing footprints, are proven and readily understood. Other reported benefits, such as improving time-to-market, lowering risk and lowering cost, still need to be realized before 3D-IC integration becomes a commercially viable alternative to traditional 2D architectures. The availability of Synopsys' silicon-proven EDA and IP solutions is an important contribution to deploying 3D-IC integration technology in the semiconductor industry."

Synopsys' 3D-IC initiative begins at the semiconductor device level. Multi-die stacks incorporate different materials, often bonded together, with varying coefficients of thermal expansion (CTE). Any temperature change causes material stress due to thermal mismatch, leading to silicon deformation and affecting transistor performance. Furthermore, TSVs, microbumps and other solder bumps produce a permanent stress in the zone around them. Synopsys' Sentaurus Interconnect TCAD tool analyzes these effects and models the TSVs in the die stacks, enabling performance and reliability optimization. Semiconductor companies, such as foundries, use modeling results to create design rules specific to 3D-IC integration to ensure manufacturability and reliability.

As part of its 3D-IC initiative, Synopsys is delivering a comprehensive EDA solution to enable design for 3D-IC integration:

- DFTMAX™ test automation: design-for-test for stacked die and TSV
- DesignWare® STAR Memory System® IP: integrated memory test, diagnostic and repair solution
- IC Compiler: place-and-route support, including TSV, microbump, silicon interposer redistribution layer (RDL) and signal routing, power mesh creation and interconnect checks
- StarRC™ Ultra parasitic extraction: support for TSV, microbump, interposer RDL and signal routing metal
- HSPICE® and CustomSim™ circuit simulation: multi-die interconnect analysis
- PrimeRail: IR-drop and EM analysis
- IC Validator: DRC for microbumps and TSVs, LVS connectivity checking between stacked die
- Galaxy Custom Designer® implementation solution: specialized custom edits to silicon interposer RDL, signal routing and power mesh
- Sentaurus Interconnect: thermo-mechanical stress analysis to evaluate the impact of TSVs and microbumps used in multi-die stacks

"The emerging 3D-IC integration technologies offer tangible benefits for design teams looking to boost system performance, reduce form factor and lower power consumption," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "2.5D- and 3D-IC integration will be key to extending the lifespan of mature process technologies and to enabling the integration of highly heterogeneous process technologies, complementing "Moore's Law" transistor scaling in many application domains. By allowing engineers to implement stacked multi-die systems more efficiently, Synopsys' 3D-IC solution can enable companies to quickly deliver innovative and advanced designs to meet the trends for faster, thinner products that use less power."

Availability
The Synopsys 3D-IC solution is available now in beta and is expected to be in production in calendar Q2 of 2012. Synopsys' 3D-IC solution will be highlighted at the Synopsys User Group (SNUG) Silicon Valley event on March 26-28, 2012.

For more information on Synopsys' 3D-IC solution, please visit: http://www.synopsys.com/3D-IC.

About Synopsys®
Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has approximately 70 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward Looking Statements
This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected availability and performance of Synopsys' 3D-IC solution. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen production or delivery delays, failure to perform as expected, product errors or defects and other risks detailed in Synopsys' filings with the U.S. Securities and Exchange Commission, including those described in the "Risk Factors" section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2011.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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